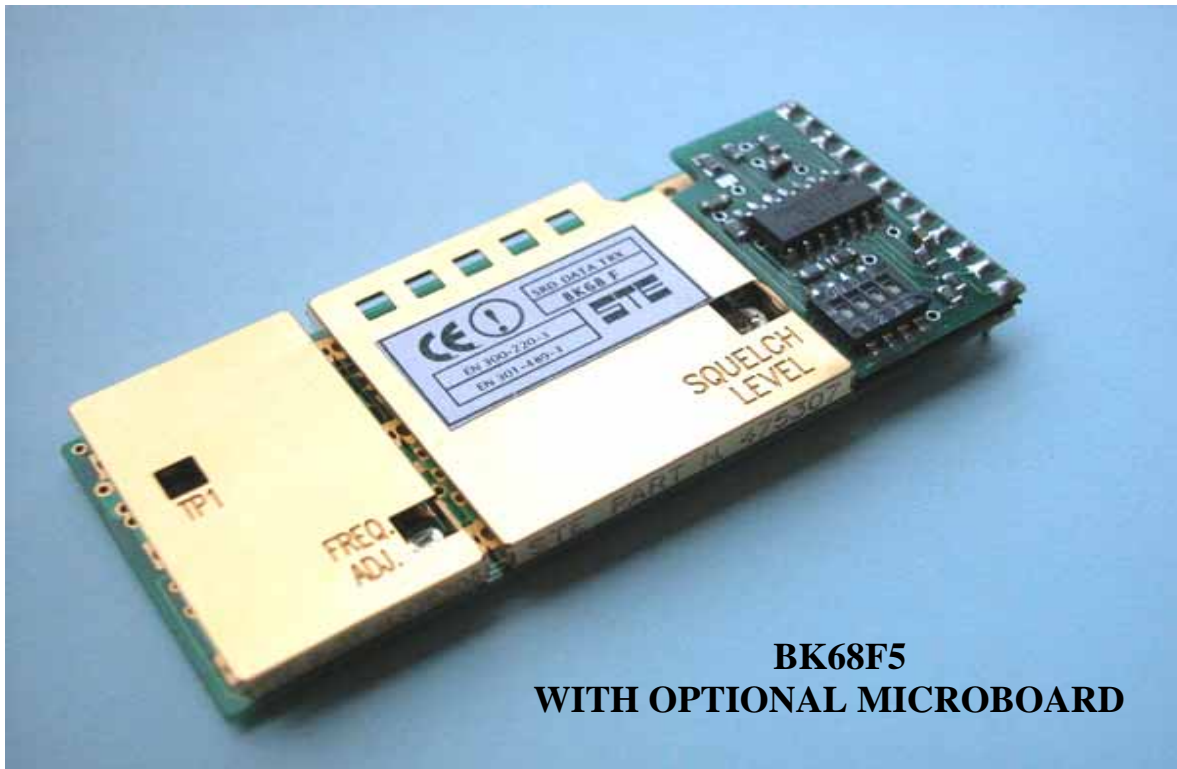


**PLL SYNTHESIZED DATA TRANSCEIVER
868 - 870 MHz ISM BAND**

BK68F5



**BK68F5
WITH OPTIONAL MICROBOARD**

OPERATING AND SERVICE MANUAL

General Description

The BK68F5 is a synthesized UHF transceiver for use in wireless data transmission applications.

The transceiver operates on the 868 – 870 MHz ISM band and it is designed to comply to the European Standards EN 300-220-3 and EN 301-489-3, in accordance with the CEPT-ERC-REC 70-03 recommendation (Annex 1 – Non Specific Short Range Devices).

Together with a precision and low phase-noise crystal controlled PLL architecture, the transceiver has high reception sensitivity (-105 dBm) and high RF output power (40 mW). High RF output power allows to employ poor efficiency antennas (helical, patch, loop or a trace on a PCB) to remain under legal 25 mW or 5mW ERP (Effective Radiated Power) limit.

The BK68F5 is designed to be directly interfaced to a microcontroller (MCU) to control and to monitor the receive and transmit mode and to program (through a 3 wires serial interface) the appropriate Rx and Tx frequencies. In a typical application the MCU manages also the communication protocol i.e. the switching between transmit and receive mode, the preamble, the start byte, the bit encoding and decoding and other important operations.

Optional microboard

An optional small μ C board (Micropic Module – part.n° 015917) can be directly mounted on the transceiver J1 connector.

The Micropic Module eliminates the necessity of an external programming of Tx and Rx frequencies. Up to 16 factory pre-programmed RF channels can be easily selected by means of a four positions dip-switch.

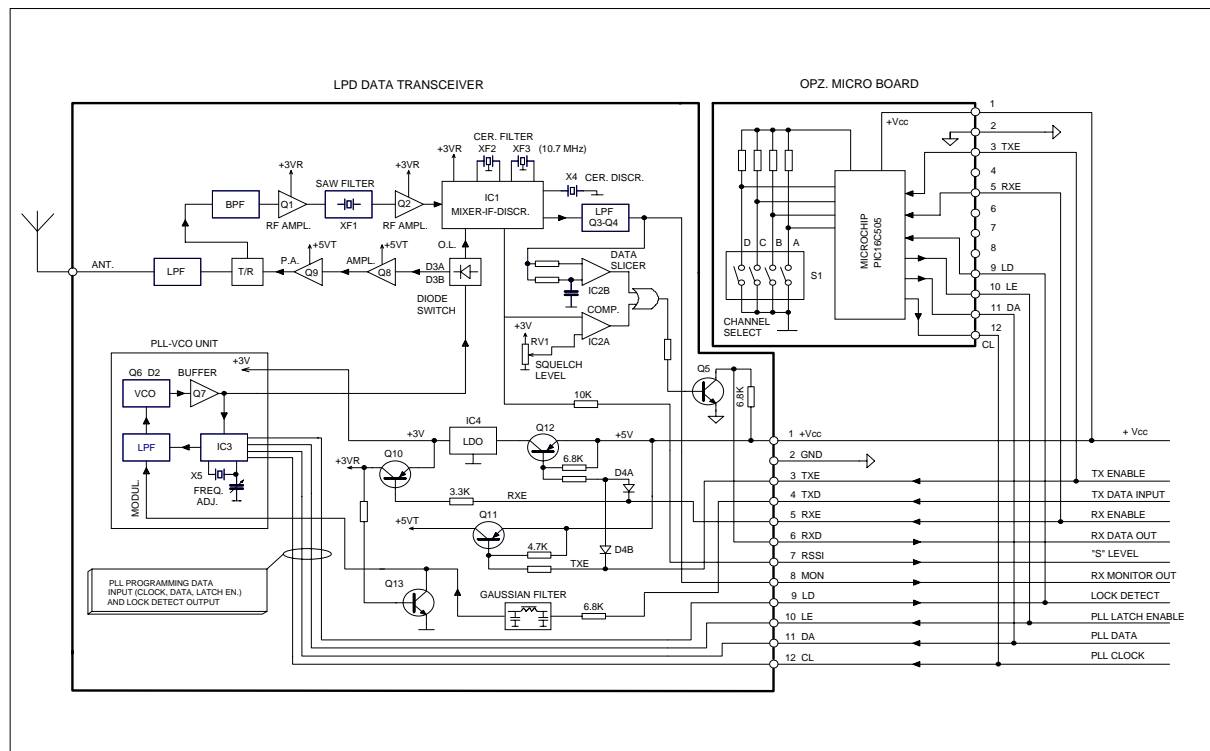


Fig.1 - Functional block diagram

BK68F5 Specifications					
	Min	Typ	Max	Units	Notes
GENERAL					
FREQUENCY RANGE	867.000		871.000	MHz	(1)
CHANNEL SPACING	150	200		KHz	
FREQUENCY PROGR. STEP	25	50	100	KHz	
FREQUENCY STABILITY		±6	±15	KHz	(2)
DATA RATE	7.2		64	Kbaud	
ANTENNA IMPEDANCE		50		Ω	
SUPPLY VOLTAGE	4.75	5	5.25	V	
SUPPLY CURRENT - SLEEP		1	10	μA	
SUPPLY CURRENT - Rx MODE		21	24	mA	
SUPPLY CURRENT - Tx MODE		40	48	mA	
OPERATING TEMPERATURE	- 20		+ 60	°C	
TRANSMITTER					
RF OUTPUT POWER	30		40	mW	(3)
SPURIOUS EMISSION			- 50	dBc	
MODULATION FREQUENCY	3.5		32	KHz	(4)
FM DEVIATION		30		KHz	(4)
R/T SWITCHING TIME		2		ms	(5)
CHANNEL SWITCHING TIME		1		ms	(5)
RECEIVER					
SENSITIVITY	- 102	- 106		dBm	
SELECTIVITY		40	30	dB	(6)
IMAGE REJECTION		50		dB	
DYNAMIC RANGE		100		dB	
SQUELCH LEVEL ADJ. RANGE	- 115	- 110	- 70	dBm	
T/R SWITCHING TIME		1.5		ms	(5)
CHANNEL SWITCHING TIME		500		μs	(5)
DIMENSIONS	57 x 24 x 4.5 mm				
WEIGHT	10 g				
<p>NOTE :</p> <p>(1) CEPT SRD BAND LIMITS = 868 - 870 MHz</p> <p>(2) OVER OPERATING TEMPERATURE RANGE</p> <p>(3) POWER ON 50 Ω . CEPT MAX ERP SUB BAND F (868 – 868,6 MHz) = 25 mW POWER ON 50 Ω . CEPT MAX ERP SUB BAND G (868,7 – 869,2 MHz) = 25 mW POWER ON 50 Ω . CEPT MAX ERP SUB BAND I (869,4 – 869,65 MHz) = 500 mW POWER ON 50 Ω . CEPT MAX ERP SUB BAND K (869,7 – 870 MHz) = 5 mW</p> <p>(4) SQUARE WAVE 0-5 Vdc LEVEL</p> <p>(5) PLL LOCK-UP TIME</p> <p>(6) AT Fo ± 200 KHz</p>					

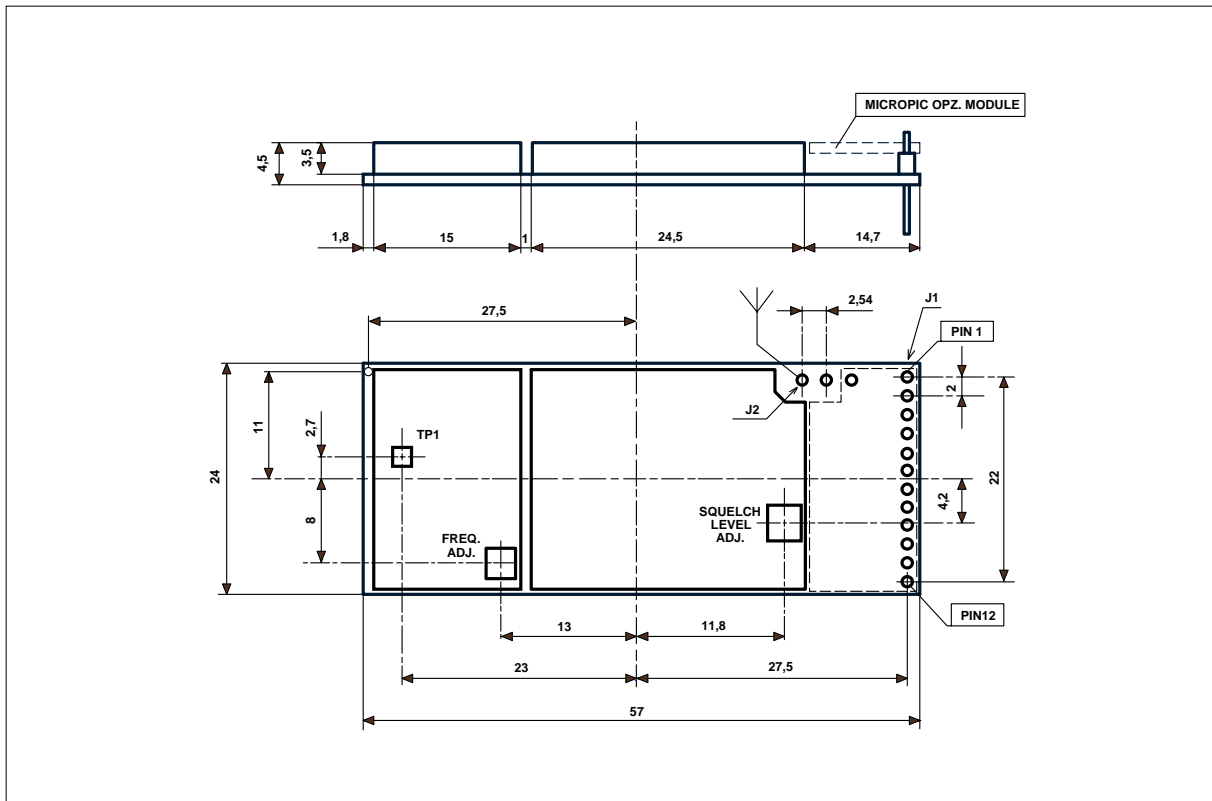


Fig. 2 - Physical dimensions

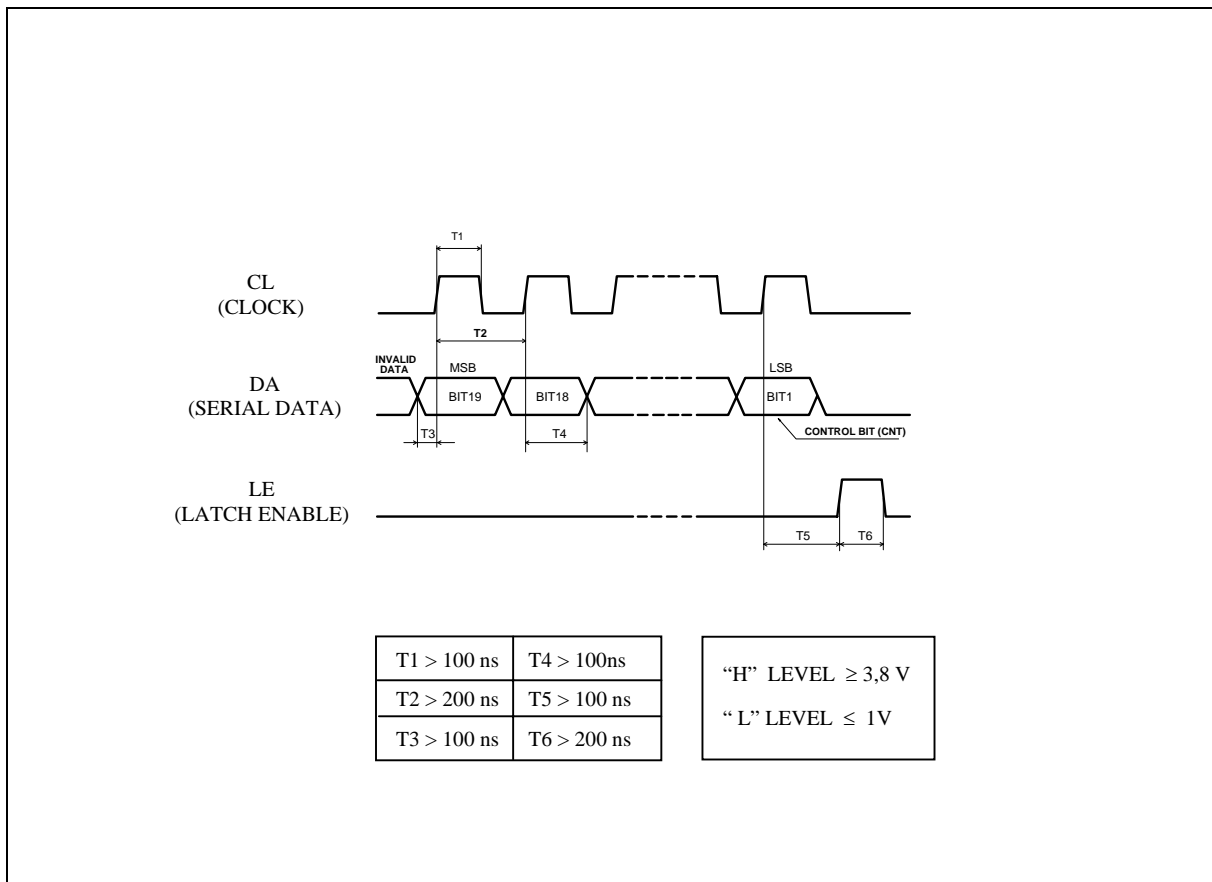


Fig. 3 - Timing diagram, serial interface.

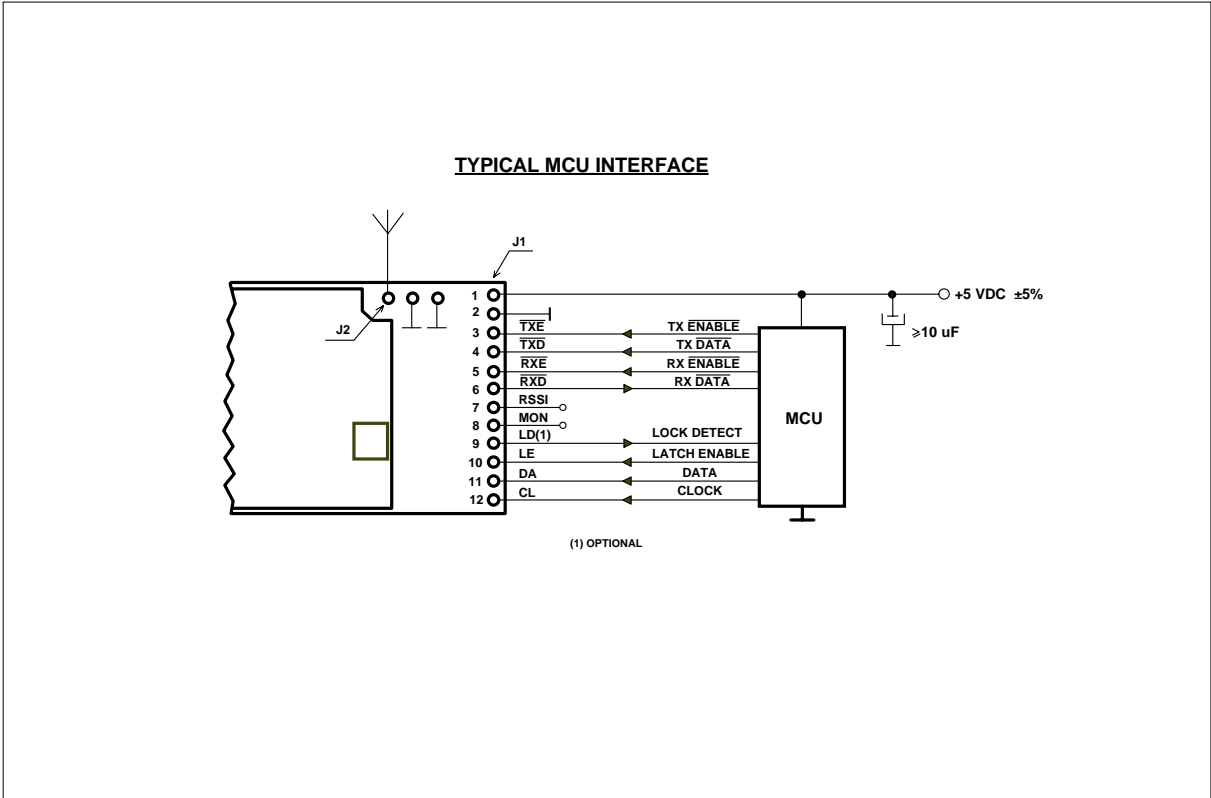


Fig. 4 - J1 pin connections.

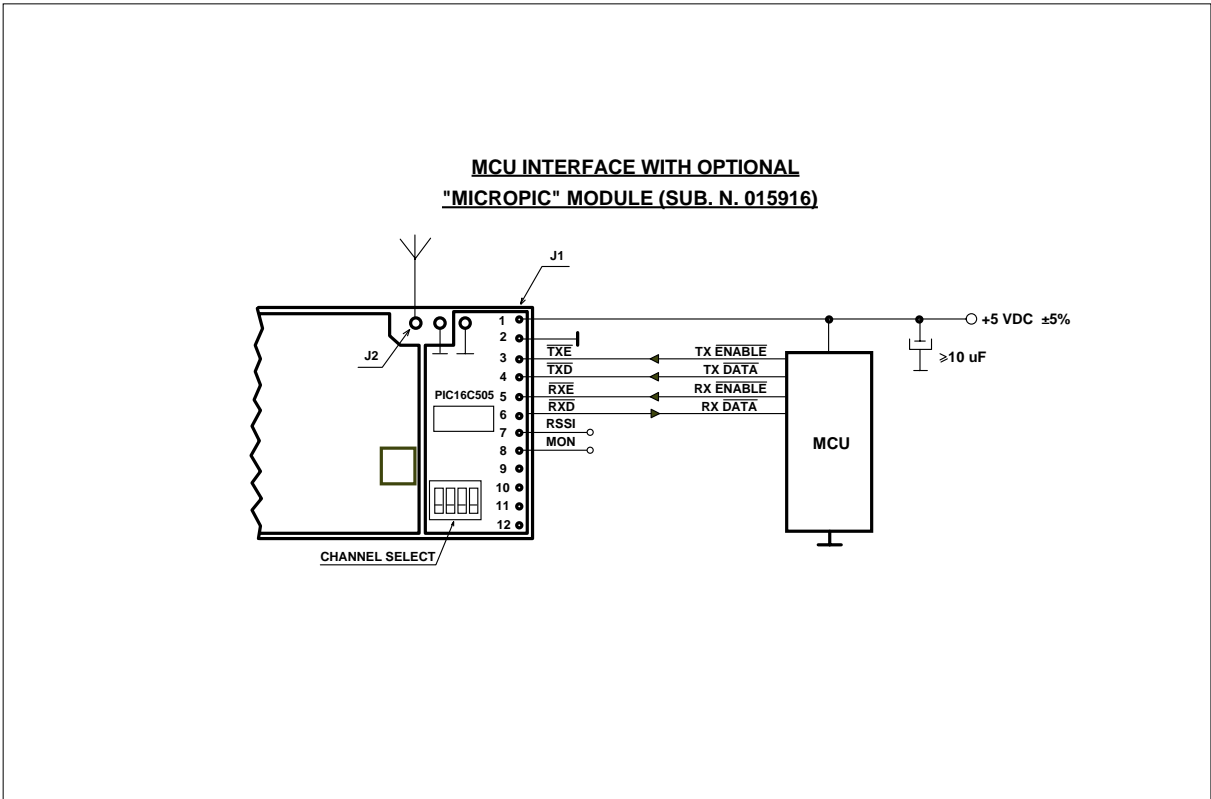


Fig. 5 - J1 pin connections

Operating modes.

The BK68F5 has three main operating modes as set by the $\overline{\text{TXE}}$ and $\overline{\text{RXE}}$ input and illustrated in table below.

MODE	TXE	RXE	DESCRIPTION
SLEEP	1	1	Quiescent current < 1 μA
RECEIVE	1	0	PLL and Receiver enabled Icc = 22 mA
TRANSMIT	0	1	PLL and Transmitter enabled Icc = 40 mA

When switched from one operating mode to another, the transceiver needs to receive, through the 3 wires serial interface, the appropriate frequency programming sets of bits.

Frequency programming.

1) The “PLL” frequency synthesizer.

Transmitter and receiver local oscillator (L.O.) frequencies are generated by a low phase-noise “VCO” (voltage controlled oscillator).

Figure 1 shows the block diagram of the transceiver.

IC3, a Fujitsu MB15E03SL, is the “PLL” integrated circuit that locks the “VCO” to the reference (X5 Xtal).

2) Serial control interface description.

A 3 wires serial control interface (clock, data and latch enable) is used to program the “PLL” IC (see fig. 6). Data are written into the 19-bit shift register at the rising edge of the “CL” (clock) signal (MSB first).

Data are transferred then into the appropriate 18-bit latch at the rising edge of the “LE” (latch enable) pulse depending on the “CNT” (control bit) value. “R” latch is loaded if “CNT” bit is set to “1”, “N” latch is loaded with “CNT” = 0.

To program a Tx or Rx frequency, two control words 19-bit length must be written into the shift register: the “R” word and the “N” word.

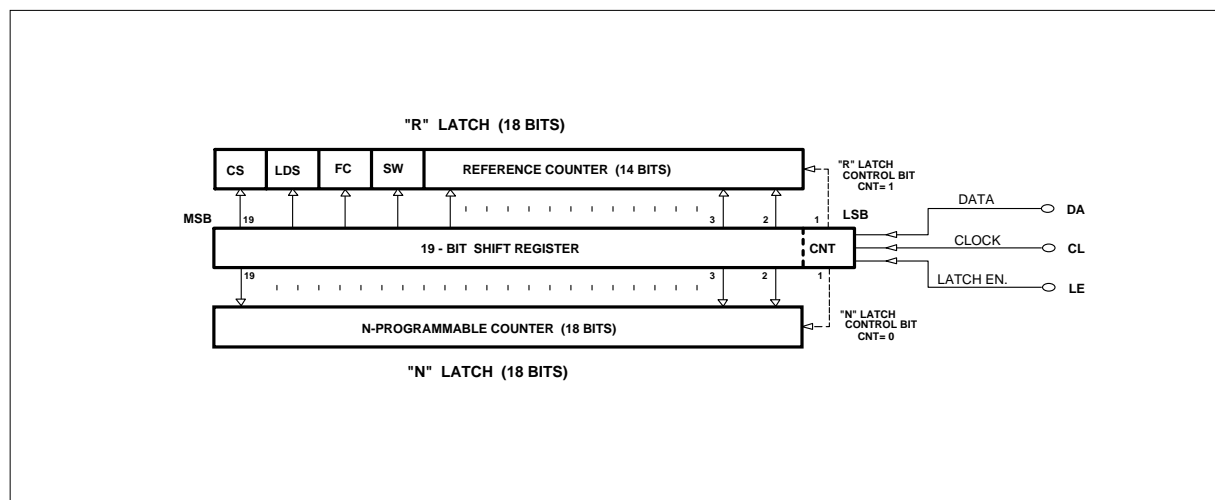


Fig. 6 - PLL internal register and latches.

3) PLL frequency synthesizer parameters

PLL IC	:	Fujitsu MB15E03SL
Reference frequency	:	16,8 MHz
Programming frequency step	:	50 KHz (recommended) 25-75-100 KHz (optional)
“SW” bit (bit 1-16 of “R” word) = 1	:	PRESCALER divide ratio = 64/65
“FC” bit (bit 17 of “R” word) = 1	:	PHASE comparator positive output
“LDS” bit (bit 18 of “R” word) = 0	:	LOCK-DETECT signal available
“CS” bit (bit 19 of “R” word) = 1	:	CHARGE/PUMP curr. = 6 mA
“CS” bit (bit 19 of “R” word) = 0	:	CHARGE/PUMP curr. = 1,5 mA

Note: Although these are the recommended parameters , different “PLL” programming modes can be implemented, if necessary. Refer to MB15E03SL data sheet at www.fujitsumicro.com for further information.

4) R-word

Bit 1 (CNT) must be set to “1”.

Bits from 2 to 15 are the “R” number

Bits from 16 to 19 are the “SW”, “FC”, “LDS” and “CS” bits.

“R” is the value that is loaded into the PLL reference divider and is calculated dividing the reference frequency (16800 KHz) by the required minimum programming frequency step.

Ex.1 : for a 50 KHz freq. step

$$R = 16800 / 50 = 336 \quad (150 \text{ H})$$

The “CS” bit is different from receive to transmit mode.

In receive mode the “CS” bit is always “1”.

In transmit mode the “CS” bit must first be set to “1” (word “R1” fast PLL lock-up time) and then, after lock-up time, must be changed to “0” (word “R2”).

For more information refer to the *timing diagrams* [pages 10 – 11].

R – WORD Examples

1

Freq. step = 50 KHz (“R” = 150H)
 “CS” = 1 (PLL charge/pump curr. = 6 mA)

R1 (50 KHz)

MSB																← SHIFT			LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
1	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0	0	0	1	
CS LDS FC SW				R										CNT					

2

Freq. step = 50 KHz (“R” = 150H)
 “CS” = 0 (PLL charge – pump curr. = 1.5 mA)

R2 (50 KHz)

MSB																← SHIFT			LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
0	0	1	1	0	0	0	0	0	1	0	1	0	1	0	0	0	0	1	
CS LDS FC SW				R										CNT					

3

Freq. step = 25 KHz (“R” = 2A0H)
 “CS” = 1 (PLL charge – pump curr. = 6 mA)

R1 (25 KHz)

MSB																← SHIFT			LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
1	0	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	
CS LDS FC SW				R										CNT					

4

Freq. step = 25 KHz (“R” = 2A0H)
 “CS” = 0 (PLL charge – pump curr. = 1.5 mA)

R2 (25 KHz)

MSB																← SHIFT			LSB
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	
0	0	1	1	0	0	0	0	1	0	1	0	1	0	0	0	0	0	1	
CS LDS FC SW				R										CNT					

3) N-word

Bit 1 (CNT) must be “0”.

Bits from 2 to 19 are the “N” number.

“N” value is calculated dividing the “VCO” frequency by the frequency step.

In transmission mode the VCO frequency is the transmit frequency . In receive mode the VCO frequency is the receive frequency minus the receiver IF (INTERMEDIATE FREQ. = 10700 KHz).

NOTE: Due to the internal architecture of the “PLL” IC , when “SW” bit of R-WORD (bit n. 16) is “1” (prescaler divide ratio = 64/65), bit n. 8 of N-word must not be used . It must be fixed to “0” and ignored.

N-WORD Examples

1

Transmit and receive freq. = 868,50 MHz

Freq. step = 50 KHz

NT (TX MODE)

$N = 868350/50 = 17367$ (43D7H)

MSB		← SHIFT (*)												LSB				
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	1	1	0
N																		CNT

NR (RX MODE)

$N = 868350 - 10700 / 50 = 17135$ (4301H)

MSB		← SHIFT (*)												LSB				
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	1	0
N																		CNT

2

Transmit and receive freq. = 868,325 MHz

Freq. step = 25 KHz

NT (TX MODE)

$N = 868325/25 = 34733$ (43D7H)

MSB		← SHIFT (*)												LSB				
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	1	0	0	0	0	1	1	1	1	0	0	1	0	1	1	0	1	0
N																		CNT

NR (RX MODE)

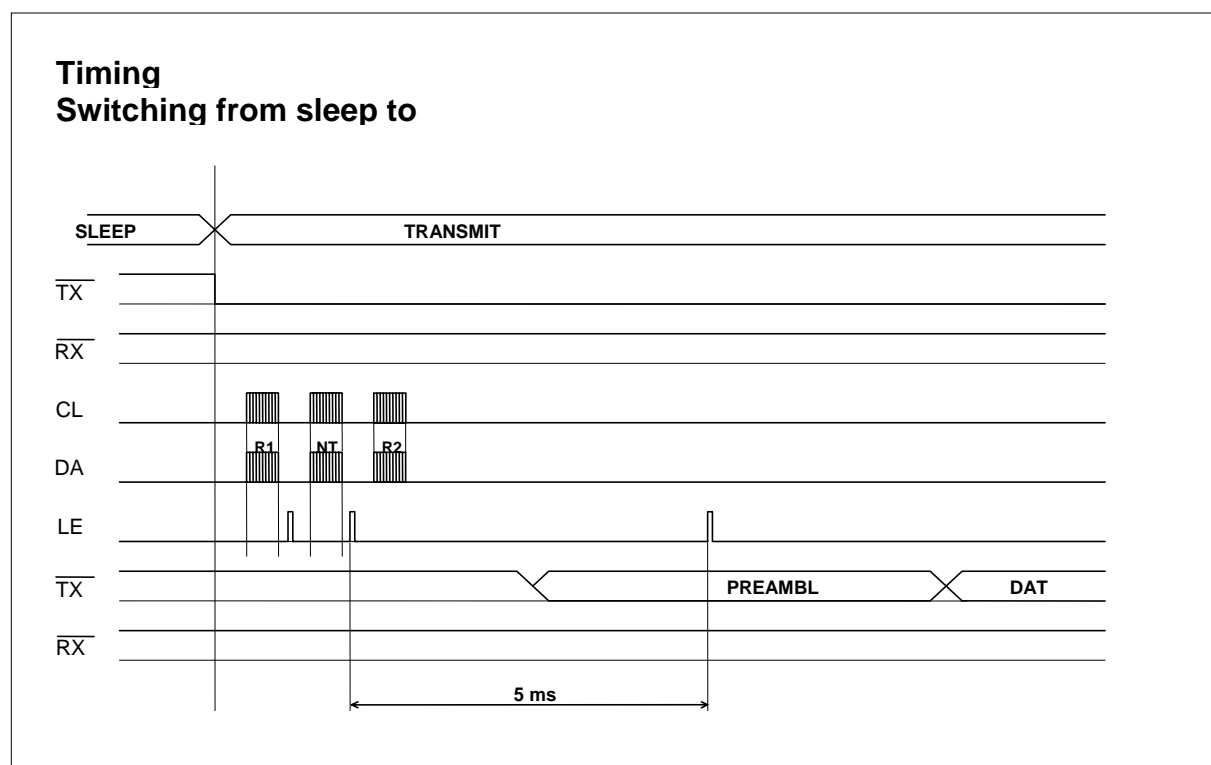
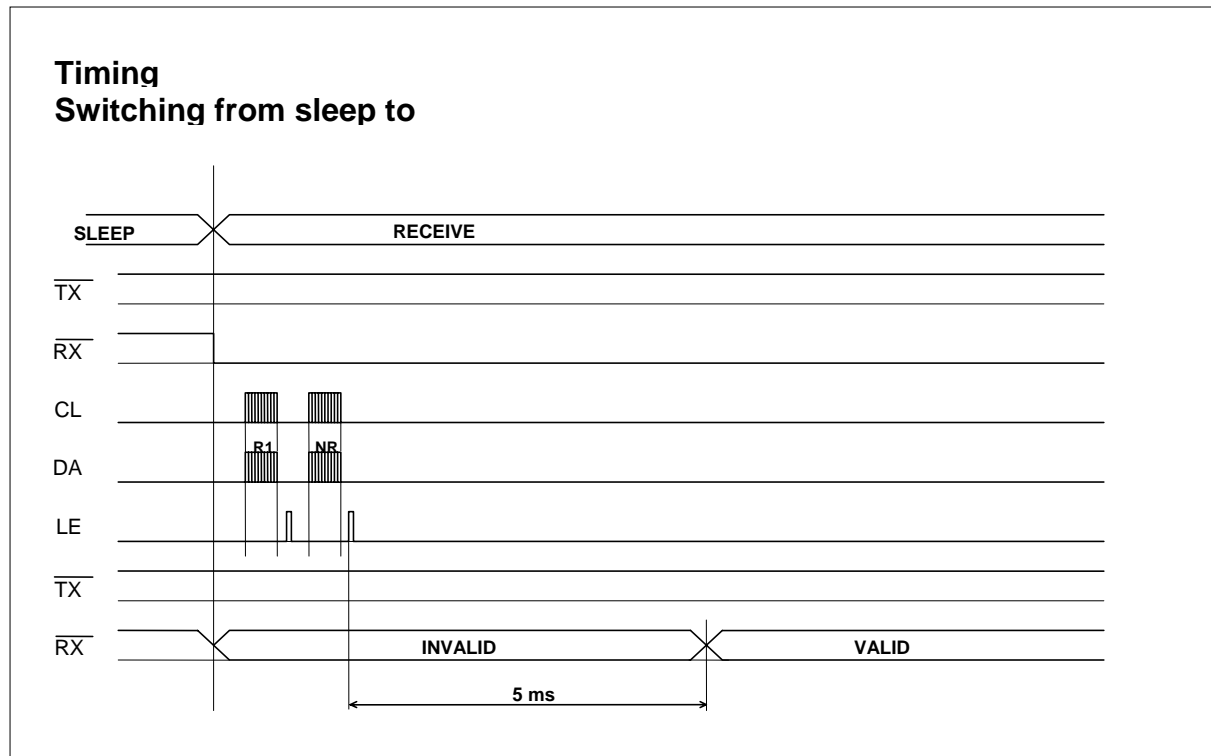
$N = 868325 - 10700 / 25 = 34305$ (8601H)

MSB		← SHIFT (*)												LSB				
19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1
0	1	0	0	0	0	1	1	0	0	0	0	0	0	0	0	0	1	0
N																		CNT

Note () : Bit n.8 is fixed to “0” and ignored.*

TIMING DIAGRAMS.

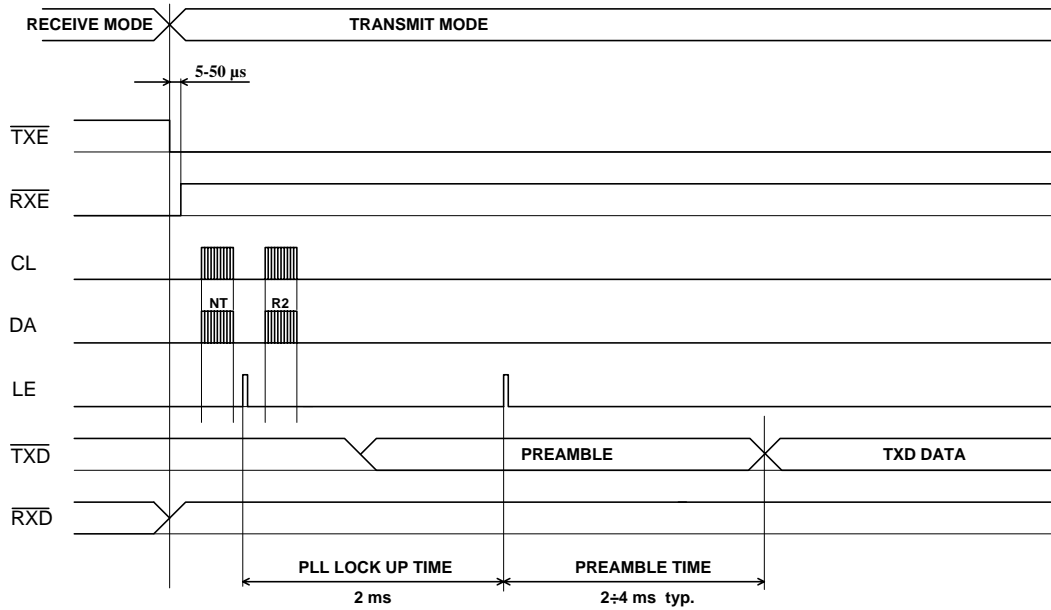
Switching between different operating modes



Note : WORD R1 and NT - Immediately after Tx enable , word R1 and NT are loaded into the 19 BIT shift register and transferred into the appropriate latch.
WORD R2 - Word R2 is loaded into the 19BIT shift register, but it is loaded into "R" latch only after PLL lock-up time.

Timing Diagram n.3

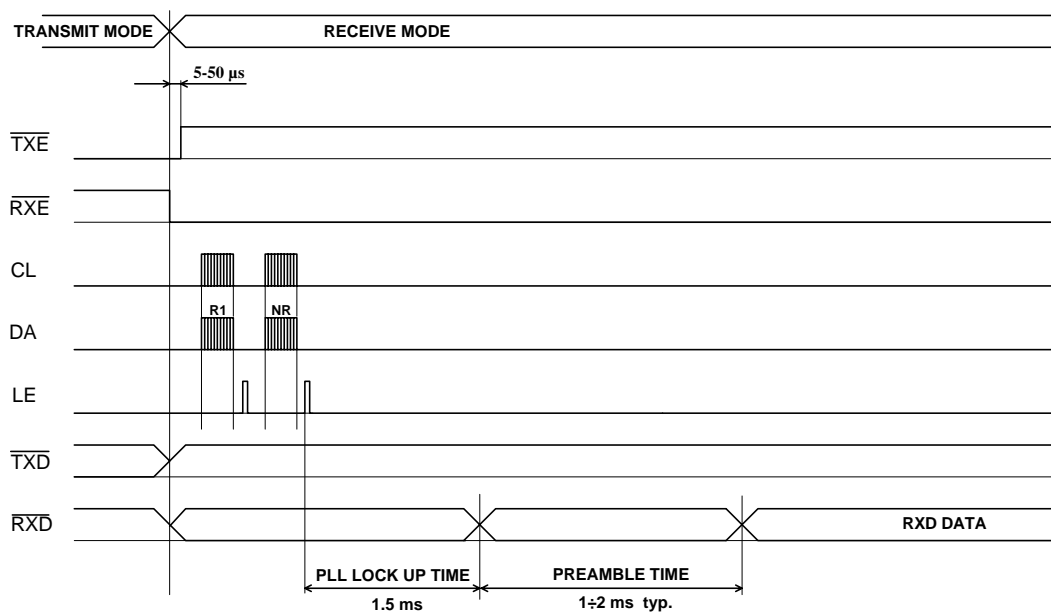
Switching from receive to transmit mode



Note : WORD NT - Immediately after Tx enable (and Rx disable), word NT is loaded into the 19 BIT shift register and transferred into "N" latch.
 WORD R2 - Word R2 is loaded into the 19 BIT shift register, but it is loaded into "R" latch only after PLL lock-up time.

Timing Diagram n.4

Switching from transmit to receive mode



Transmitter data input (TXD – J1 pin n. 4).

TXD input (negative logic) will accept serial digital data with a 0 V to 5 V level (for full Tx modulation). Modulation shaping is performed by a Gaussian low pass filter to minimize spectral spreading (see fig. 1).

Bit-rate is upper limited by the cut-off frequency of the low-pass filter.

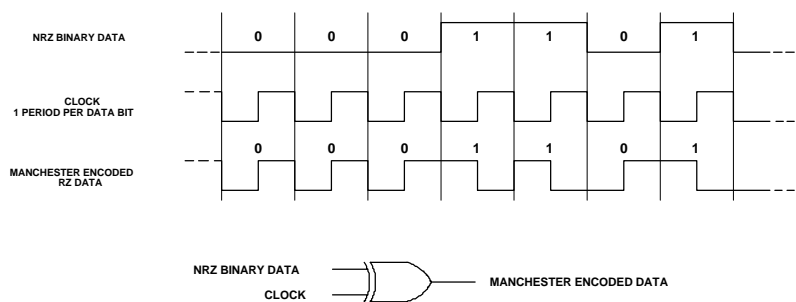
Minimum bit-rate depends on the “PLL” loop filter time constants and the value of “CS” bit (R-word). Minimum acceptable square wave modulation frequency is 3 KHz (with “CS” bit = 0), DC levels or a data /streams with DC unbalance are prohibited.

Bi-phase “RZ” coding schemes (differential bi-phase or Manchester code) are recommended to eliminate any DC component that depends on the bit pattern.

MESSAGE ENCODING

Code modification , Manchester style , means combining a clock with the data to give two bits of output data for any single input bit.

Recommended clock frequency is 4,8 KHz to 19,2 KHz (maximum clock frequency is 38,4 KHz).



Received data output (RXD - J1 pin n. 6).

RXD (negative logic) is an open collector output (Q5 transistor – fig. 1) with a pull-up resistor to Vcc.

The received data stream demodulated by IC1 discriminator goes to a post detection low pass filter (Q3 - Q4) which limits the signal bandwidth and ensures the clean operation of the subsequent self-centering data slicer (IC2B).

A squelch circuit , blocks the RXD output when the received signal strenght falls a preset value (adjusted by RV1).

The squelch level is factory preset with to approx. 6 dB under max. sensitivity. RV1 can be adjusted to increase the squelch level threshold.

This adjustment is best performed in laboratory with a calibrated RF generator.

It is also possible to adjust RV1 observing the received RF signal level on “RSSI” output .

MESSAGE DECODING

On the receiver side, transmitted (bi-phase encoded) datas, must be extracted from noise, interference and multipath propagation distortions.

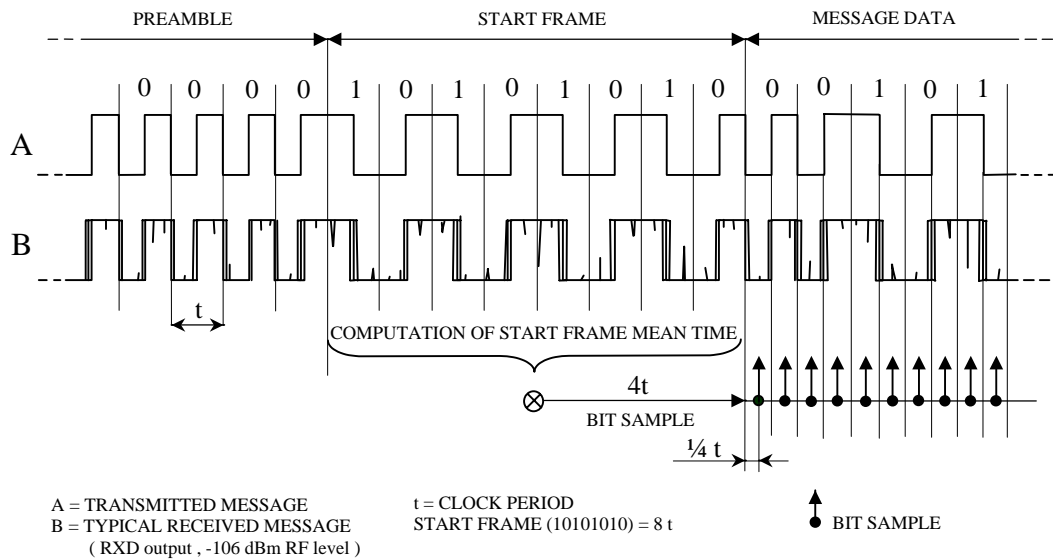
It is very instructive, before any decode attempt, to examine the received datas as appear on the “MON” analog output.

A good system is to employ as a beacon a transceiver module in transmit mode, modulated by a square-wave (clock frequency) and to simulate all the steady and transitory situations of a real message exchange.

Suppose transmitted data are Manchester encoded , as described in the previous example. It will be necessary to send a preamble, a synchronization frame and then the message .

The preamble is only to allow Tx and Rx to stabilize on the frequency and to centre modulation and data slicer.

The synchronisation frame is to be used to define start point for following bits decoding.



In the above example , if “ t ” is the clock period, the total length of the eight bits start frame (10101010) is “ 8 t “.

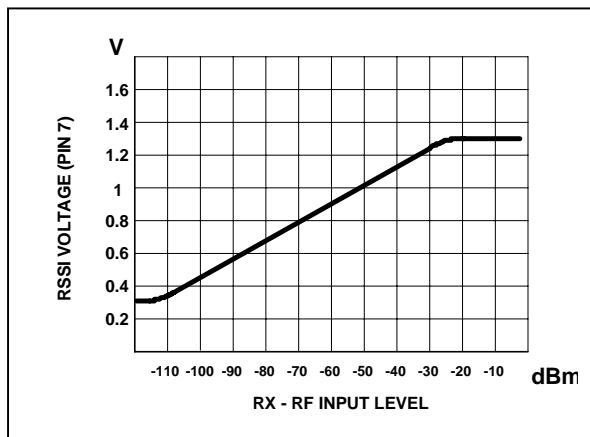
The start frame must be extracted from a noisy reception detecting the rising and falling edge of the received message.

Once extracted from the received noisy signal , the 8 bits of the start frame can be averaged on the total frame time to permit to define the data message start point. The following message data bits are best decoded sampling two times every bit.

- Note:
- Obviously any tolerance in the Rx and Tx clock frequency must be taken in consideration and related to the total message bit number.
 - Control and validation of the message together with error correction algorithms, message retry request, etc. is a task to be performed by the “ packet” protocol.

Received signal strength indicator output (RSSI – J1 pin n. 7).

RSSI is a received signal strength output with more than 90 dB dynamic range (fig. 7).



dBm to RF Volt conversion $Z_0 = 50\Omega$ 0 dBm = 1 mV			
dBm	RF mV	dBm	RF μ V
-20 dBm	22,4 mV	-80 dBm	22,4 μ V
-30 dBm	7,07 mV	-90 dBm	7,07 μ V
-40 dBm	2,24 mV	-100 dBm	2,24 μ V
-50 dBm	0,70 mV	-110 dBm	0,7 μ V
-60 dBm	0,22 mV	-120 dBm	0,22 μ V
-70 dBm	0,07 mV	-130 dBm	0,07 μ V

Fig. 7 - RSSI output.

The accurate "RSSI" output can be used to test and evaluate antenna performances and to measure radio waves propagation and attenuation.

Monitor analog Rx output (MON – J1 pin n. 8).

This is a direct analogue output from demodulator.

It is employed during receiver test, but it is also very useful during system test to observe (before shaping) the received signal. This will help to evaluate the signal to noise ratio and the signal distortion as for example influenced by radio waves propagation anomalies (multipath reflection).

The monitor output can also be of great help to detect and observe noise and interference sources (for example from micros , fast logic IC , noisy diodes or zeners etc.). A small loop at the end of a coaxial 50 Ω cable and connected to antenna input can help to measure and locate suspect noise sources.

Lock detect output (LD –J1 pin n. 9).

During normal operation, in receive or transmit mode , the “ PLL” is locked to the correct programmed frequency and the LD output is high (+3 V).

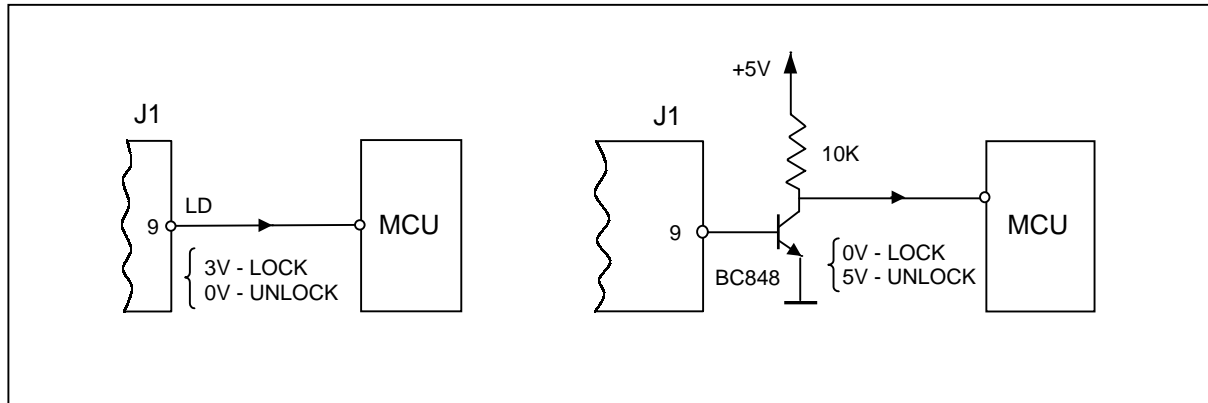
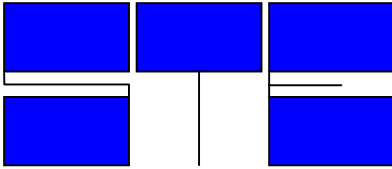


Fig. 8 Lock detect output interface to MCU.

During normal operation, with short transmission and reception periods, it is not usually necessary to control the “UNLOCK” situation.

An “UNLOCK” situation is possible during a long period of continuous transmission (usually prohibited) or reception : in this case the MCU detects the “UNLOCK” state and provides to resend the appropriate programming words.

Note : Avoid to sample the “LD” status immediately after the programming sequence. A time of 100 ms or more , also between subsequent “LD” controls , is recommended.



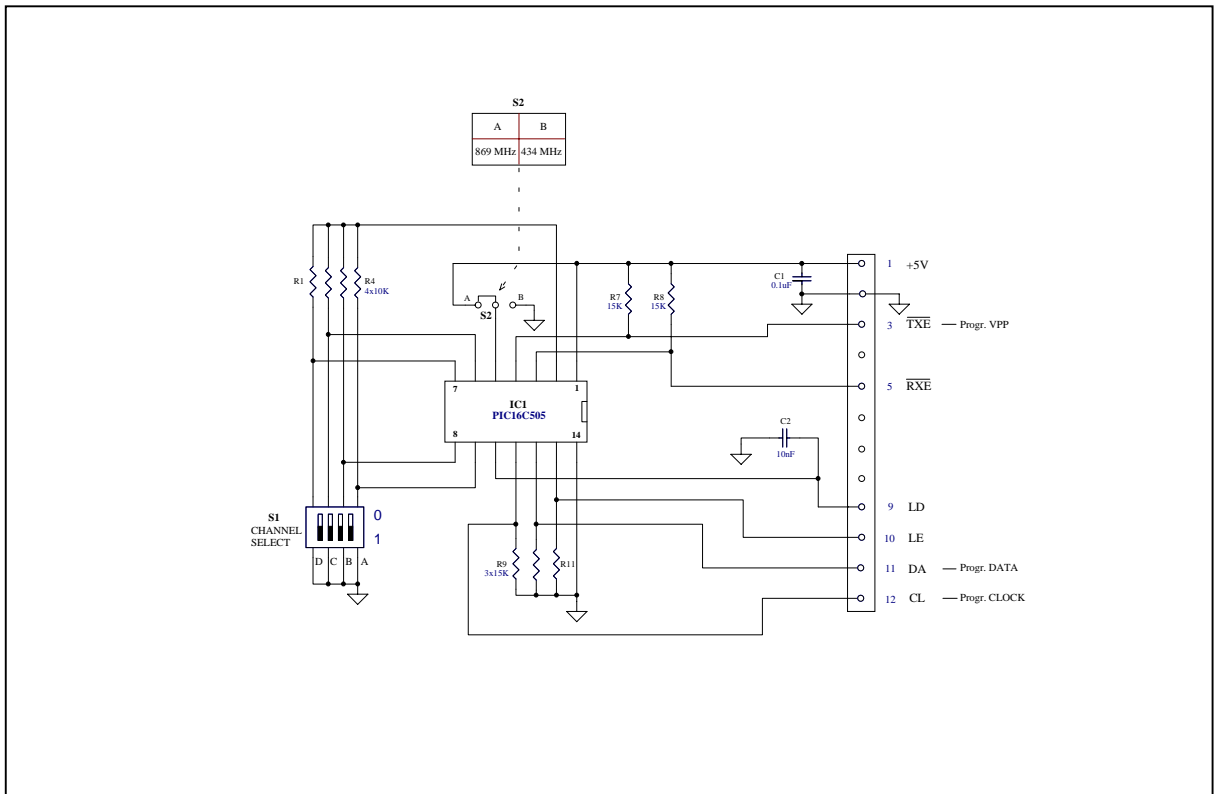
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MICROPIC MODULE

The optional Micropic Module can be directly mounted on BK67, BK68 and BK69 data transceiver.

The on board microcontroller (PIC16C505) programs the transceiver, through the serial data interface on 16 different radio channels as selected by S1 (a four position dip – switch).

The microcontroller also samples every 100 ms the LD (lock detect) output to monitor the “PLL” status , reprogramming the transceiver in case of “unlock” event.



Antennas

In transmission the antenna allows RF energy to be efficiently radiated into free space.

Note 1 : the BK6X output RF power is purposefully set higher than the legal limit. This allows to utilize a poor efficient antenna to radiate max legal power.

In reception the antenna intercepts the electromagnetic RF field (an equivalent capture area is defined for every antenna) and sends the resulting weak current to the receiver input.

Note 2 : the receiving antenna should capture as much of the transmitted signal as possible and as little as possible of other undesired signals.

Note 3 : it is useless to have a high RX sensitivity and the good antenna located very near to disturbing sources like fast logic circuits, switching power regulators, etc.

There are hundreds of antenna styles and variations that may be employed (dipole, whip, helical, spiral, loop, patch, etc.) but the simplest and most popular antenna is the quarter wavelength whip antenna (ground-plane antenna).

Basically the ground-plane “whip” antenna is quarter wavelength wire that stands above ground-plane.

This antenna is very simple to design and to manufacture, but to be successful it is necessary to match two conditions:

- 1°) The wire (the radiating element) must stand right in open space, perpendicular to ground-plane and far away from conductive obstacles (metal parts – walls – etc.).
- 2°) The ground-plane must be really “ground” , i.e. it must have enough extension compared to wavelength to be really “zero” equipotential ground.

Note 4 : the ground-plane antenna has (at resonance frequency) nominal impedance of 36 Ω , which is close enough to standard 50 Ω impedance.