

## General Description

The BCT2614S is a frequency synthesizer digital PLL chip used for electronic tuning by AM & FM DTS radios with supply voltage from 3.6V down to 1.8V. The BCT2614S is made using advanced CMOS process for low voltage, low power and low radiation operations.

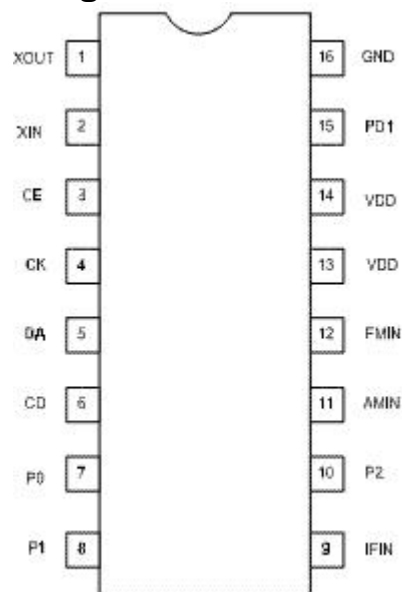
## Features

- Low supply voltage: from 1.8 to 3.6V
- High speed programmable frequency divider
  - FMIN : 10 to 180 MHz
  - AMIN : 2 to 40MHz Pulse Swallow  
0.4 to 10MHz Direct Division
  - IFIN : 0.4 to 12 MHz
- Seven Reference Frequency Selectable:  
1 kHz, 3 kHz, 3.125 kHz, 5 kHz, 6.35 kHz,  
12.5 kHz and 25 kHz.  
( reference to 75kHz low radiation oscillator)
- Three State Phase Detector: with Built-in  
unlock detection circuit
- 3 Dedicated Output Ports
- 3 Wire Serial Data Input : CE, CK and DA
- Pb-free SO16L package

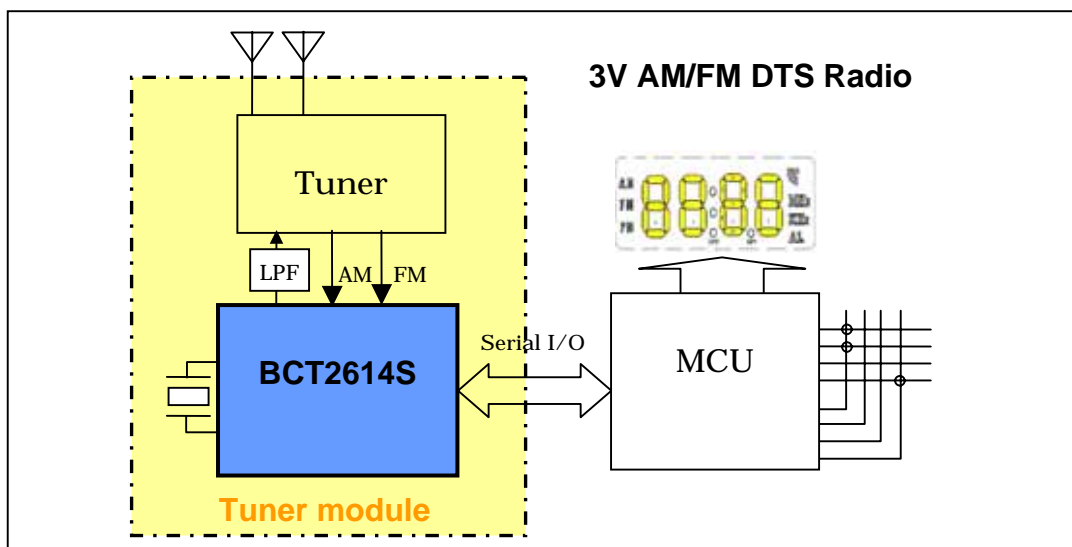
## Applications

- AM / MW / FM radio tuner
- Radio tuner module
- PLL frequency synthesizers

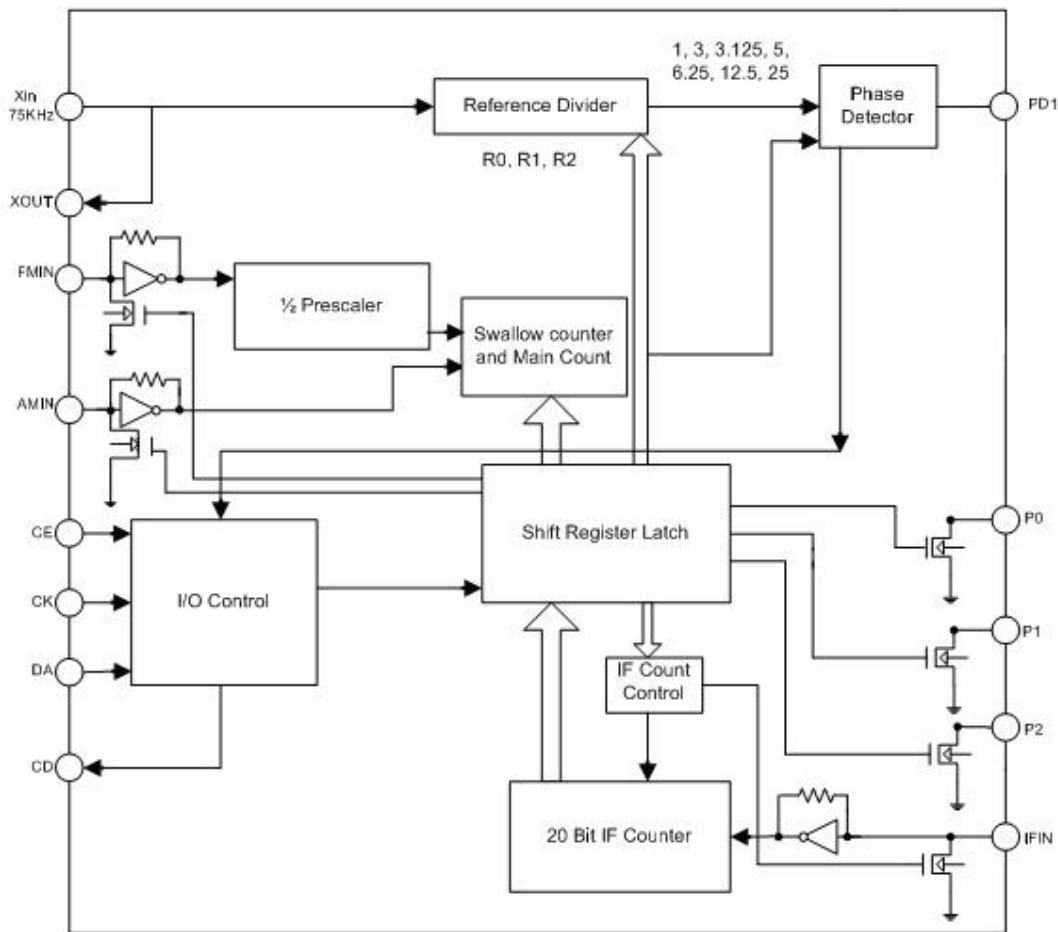
## Package



## Typical Application Circuit



## Block Diagram



## Absolute Maximum Specifications

Rating	Symbol	Value	Unit
Supply voltage range	$V_{DD}$	-0.3 to +4.5	Volts
Input voltage range	$V_{IN}$	-0.3 to $V_{CC}+0.3$	Volts
Output voltage range	$V_{OUT}$	-0.3 to $V_{CC}+0.3$	Volts
Operating temperature range	$T_{OPR}$	0 to 70	°C
Storage temperature range	$T_{STR}$	-20 to 100	°C

## Pin Descriptions

Pin Number	Pin Name	I/O	Description
2	XIN	Input	75 kHz Oscillator Input Pin
1	XOUT	Output	75 kHz Oscillator Output Pin
3	CE	Input	When CE is High, DA is synchronous with the rise of CK and read to the internal shift register. DA is then latched at the falling edge of CE. Data is output on CD synchronous to rising edge of CK
4	CK	Input	
5	DA	Input	
6	CD	N-Channel Open Drain Output	Count Data : Frequency data and unlock data are output on CD
7, 8, 10	P0, P1, P2	N-Channel Open Drain Output	General Purpose Output Ports
9	IFIN	Input	Intermediate Frequency input – for Frequency measurement
12	FMIN	Input	FM Input
11	AMIN	Input	AM Input
15	PD1	Tri-State Output	Phase Comparator Output: 'H' when value obtained by dividing local output is higher than standard frequency 'L' when value is lower 'Z' when value is same
14	VDD	Power	Power supply 1.8V to 3.6V
13	VDD	Power	Power supply 1.8V to 3.6V
16	GND	Ground	Ground

## Electrical Specifications

All electrical specifications are specified at  $T_{AMBIENT}$  from 0 °C to 70 °C,  $V_{CC}$  from 1.8 volts to 3.6 volts, unless otherwise specified.

## DC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
$V_{DD}$	Chip Supply Voltage	$V_{DD1}$ and $V_{DD2}$	1.8	3.0	3.6	Volts
$I_{DD}$	Power Supply Current	$V_{DD}$ , $F_{MIN} = 130\text{MHz}$ , 50mVp-p		6	12	mA
$I_{DD14}$	Power Supply Current (pin 14)	$V_{DD1}$		3	6	mA
$I_{DD13}$	Power Supply Current (pin 13)	$V_{DD2}$ , $F_{MIN} = 130\text{MHz}$ , 50mVp-p		3	6	mA
$I_{DDSTB}$	Quiescent Current	No Input, PLL = OFF		30	60	$\mu\text{A}$
$V_{IL}$	Input Voltage Low	CE,CK and DA	0		0.5	Volts
$V_{IH}$	Input Voltage High	CE,CK and DA	$V_{DD} - 0.5$		$V_{DD}$	Volts
$I_{IL1}$	Input Current Low	CE,CK and DA	-1			$\mu\text{A}$
$I_{IH1}$	Input Current High	CE,CK and DA			1	$\mu\text{A}$
$I_{ILXIN}$	Input Current Low for XIN	XIN		-0.3		$\mu\text{A}$
$I_{IHXIN}$	Input Current high for XIN	XIN		+0.3		$\mu\text{A}$
$V_{OL}$	Output Voltage Low	$P_0, P_1, P_2, CD$ $I_{OL} = 1\text{mA}$		0.2	0.5	Volts
$V_{OLOFF}$	Output Voltage Low at FMIN, AMIN and IFIN	When OFF, $I_{OL} = 0.1\text{mA}$			0.5	Volts
$V_{OLPD1}$	Output Voltage Low for PD1	PD1, $I_{OL} = 1\text{mA}$		0.5	1.0	Volts
$V_{OHPD1}$	Output Voltage High for PD1	PD1, $I_{OH} = -1\text{mA}$	$V_{DD} - 1.0$	$V_{DD} - 0.3$		Volts
$I_{ILPD1}$	Input Leakage Low for PD1 when in Hi Z State	PD1, $V_{IN} = V_{DD}$			100	nA
$I_{IHPD1}$	Input Leakage High for PD1 when in Hi Z State	PD1, $V_{IN} = V_{SS}$	-100			nA

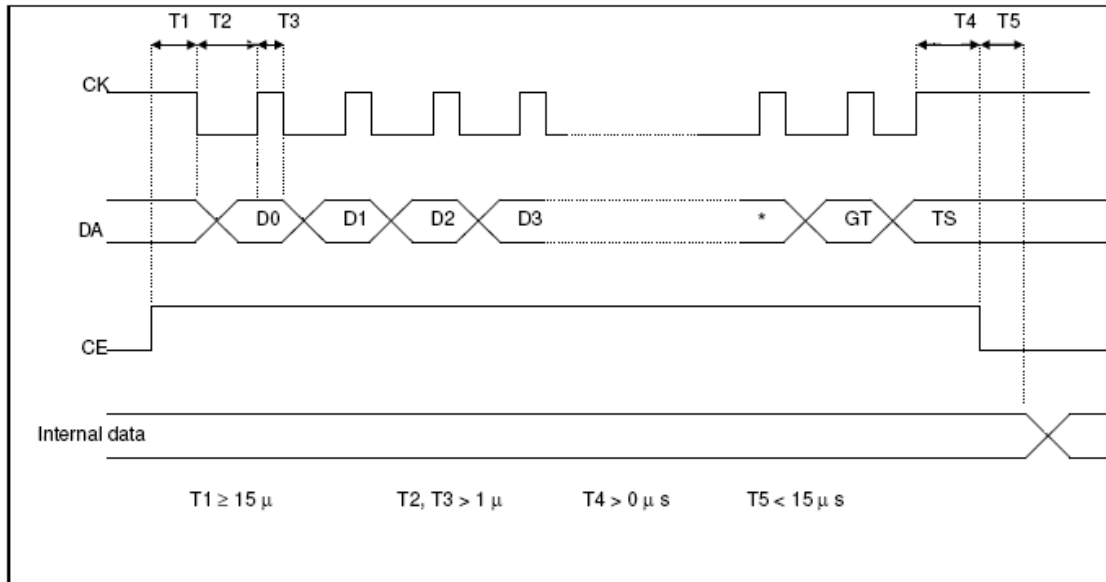
## AC Specifications

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
F <sub>FMIN</sub>	Input Frequency for FMIN	FMIN, 140mVp-p Sinusoidal waveform, AC Coupled	10		180	MHz
F <sub>AMIN</sub>	Input Frequency for AMIN	AMIN, 40mVp-p Sinusoidal waveform, AC Coupled	0.4		40	MHz
F <sub>IFIN</sub>	Input Frequency for IFIN	IFIN, 140mVp-p Sinusoidal waveform, AC Coupled	0.4		16	MHz
S <sub>FMIN</sub>	Input sensitivity for FMIN	FMIN below 130MHz Sinusoidal waveform, AC Coupled	140			mVp-p
S <sub>AMIN</sub>	Input sensitivity for AMIN	AMIN below 5MHz Sinusoidal waveform, AC Coupled	40			mVp-p
S <sub>IFIN</sub>	Input sensitivity for IFIN	IFIN below 12MHz Sinusoidal waveform, AC Coupled	140			mVp-p
t <sub>PW</sub>	Minimum Pulse Width	CK and DA	1			μs
T <sub>rise</sub>	Rise Time	CE, CK, and DA			500	ns
T <sub>fall</sub>	Fall Time	CE, CK, and DA			500	ns

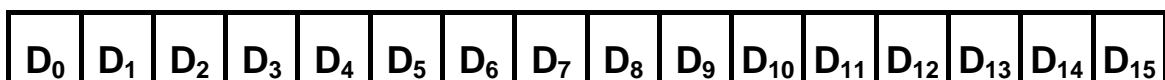
**Detailed Circuit Description:**

**Serial I/O**

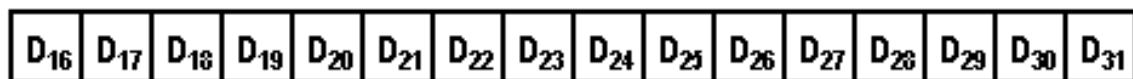
**Input Data Format**



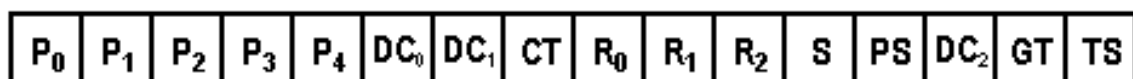
An internal reset is generated on rising edge of CE to reset internal counters. A minimum of (T1) 15 Microseconds is required for this purpose. Input data is sampled on rising edge of CK and finally latched into internal register when the CK pulse count has reached 32. "0" should be programmed on all reserved bits.



For explanation of D<sub>0</sub> ~D<sub>15</sub>, please go and refer to Part B.4.1



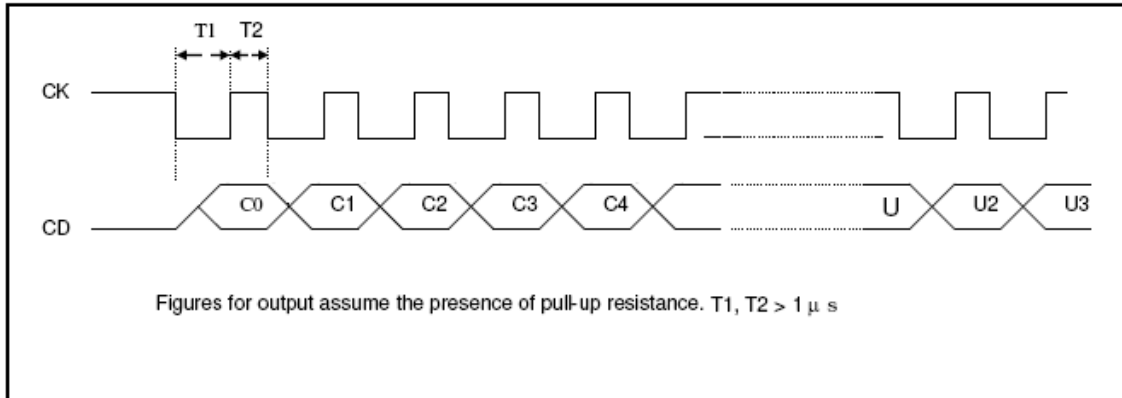
← Input done from D<sub>16</sub>



Corresponding register bit

### Output Data Format

Data is output on CD on the falling edge of CK while CE is low.



C <sub>0</sub>	C <sub>1</sub>	C <sub>2</sub>	C <sub>3</sub>	C <sub>4</sub>	C <sub>5</sub>	C <sub>6</sub>	C <sub>7</sub>	C <sub>8</sub>	C <sub>9</sub>	C <sub>10</sub>	C <sub>11</sub>	C <sub>12</sub>	C <sub>13</sub>	C <sub>14</sub>	C <sub>15</sub>
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← Input done from C<sub>0</sub>

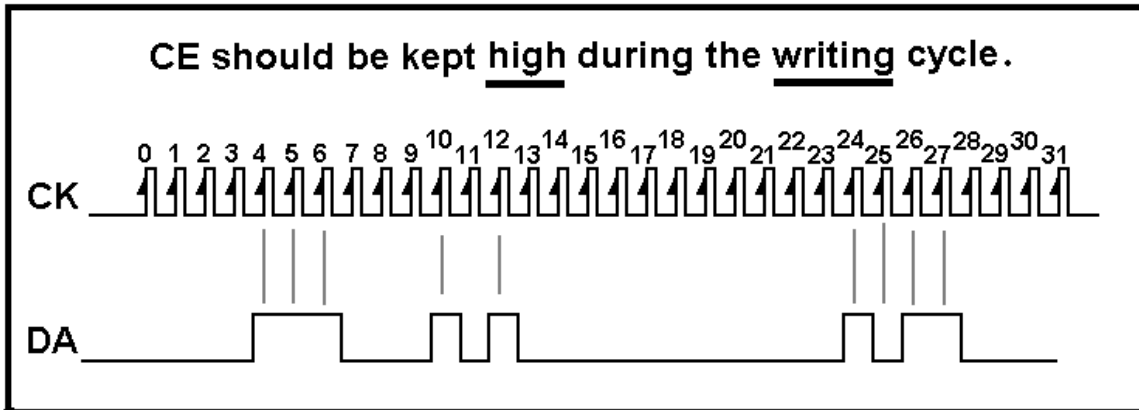
C <sub>16</sub>	C <sub>17</sub>	C <sub>18</sub>	C <sub>19</sub>	U <sub>0</sub>	U <sub>1</sub>	U <sub>2</sub>	U <sub>3</sub>
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Data output possible when CT=1 or GT = 1

**Explanation of the data**

- (1) Input data format (writing instructions) to PLL chip :  
From D0 to D15, data can be calculated in accordance with following examples. (When S=1, use D4 through D15 only.)

First example:



S=1, PS=0; Standard frequency=3KHz Input Data= 1470H

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
X	X	X	X	1	1	1	0	0	0	1	0	1	0	0	0
<b>Don't care</b>				<b>7</b>				<b>4</b>				<b>1</b>			

147H = 327 (decimal);

Target oscillation frequency = (327 x 3) KHz = 981KHz

If the IF frequency is 450KHz, the radio carrier frequency will be 531KHz for the single superheterodyne application.

Second example:

S=0; Standard frequency = 25KHz Input Data= 07ACH

D <sub>0</sub>	D <sub>1</sub>	D <sub>2</sub>	D <sub>3</sub>	D <sub>4</sub>	D <sub>5</sub>	D <sub>6</sub>	D <sub>7</sub>	D <sub>8</sub>	D <sub>9</sub>	D <sub>10</sub>	D <sub>11</sub>	D <sub>12</sub>	D <sub>13</sub>	D <sub>14</sub>	D <sub>15</sub>
0	0	1	1	0	1	0	1	1	1	1	0	0	0	0	0
<b>C</b>			<b>A</b>				<b>7</b>				<b>0</b>				

7ACH = 1964 (decimal);

Since the whole divider value is 2n for S=0 where n=1964, the internal processing divider value becomes 1964 x 2 = 3928

Target oscillation frequency = (3928 x 25) KHz = 98.2MHz

If the IF frequency is 10.7MHz, the radio carrier frequency will be 87.5MHz for the single superheterodyne application.

- (2) CT : Frequency measurement beginning data  
 1: Begins measurement.  
 0: Resets internal counter, IFIN go to pull down.

- (3) Output port control data: P<sub>0</sub>, P<sub>1</sub>, P<sub>2</sub>  
 1: Open Drain output ON.  
 0: Open Drain output OFF.

These ports are designed to has no logic glitch when same value are programmed from the serial I/O

- (4) R<sub>0</sub>, R<sub>1</sub>, R<sub>2</sub>, standard frequency data

Data			Standard Frequency	75kHz Ratio
R <sub>0</sub>	R <sub>1</sub>	R <sub>2</sub>		
0	0	0	25 kHz	1/3
0	0	1	12.5 kHz	1/6
0	1	0	6.25 kHz	1/12
0	1	1	5 kHz	1/15
1	0	0	3.125 kHz	1/24
1	0	1	3 kHz	1/25
1	1	0	1 kHz	1/75
1	1	1	*PLL OFF	

- *FMIN = pull down, AMIN = pull down, PD1 = high impedance*

- (5) S: Switch between FMIN and AMIN      '0': FMIN, '1': AMIN

S	FMIN	AMIN
0	Activated	Deactivated, input pulled down
1	Deactivated, input pulled down	Activated

- (6) PS: (Prescaler Select) If this bit is set to “1”, while AMIN is selected, swallow counter division is possible.

Input pin	S	PS	Dividing mode	Input Frequency Range	Divider
AMIN	1	0	Direct dividing	0.4 ~ 20MHz	n
	1	1	Pulse swallow	3 ~ 40MHz	n
FMIN	0	x	½ + Pulse swallow	60 ~ 180MHz	2n

x: Don't care

- (7) GT: Frequency measurement time and unlock detection ON/OFF.

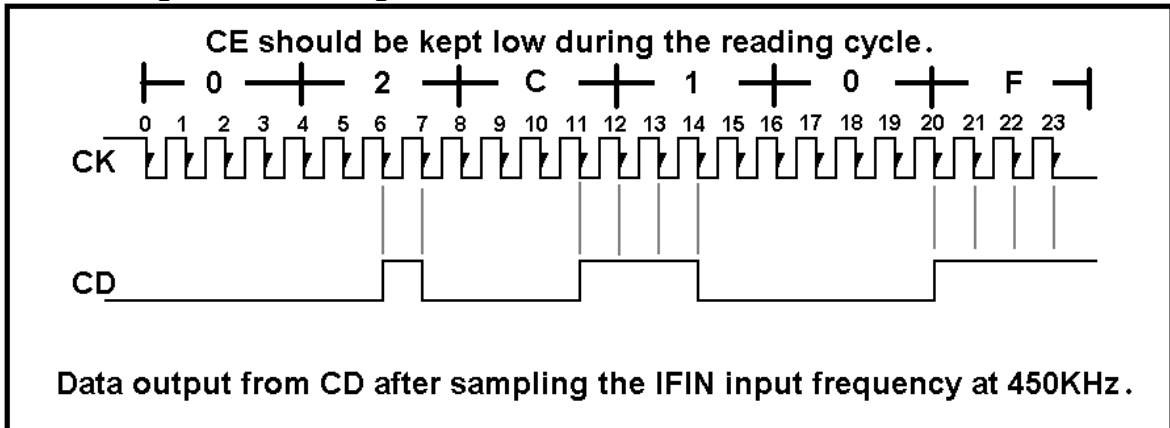
CT	GT	Frequency measurement	Unlock detection	Data output
0	0	OFF	OFF	NG
0	1	OFF	ON	OK
1	0	ON Gate time = 16 ms	ON	
1	1	ON Gate time = 32 ms	ON	

- (8) TS: Test data (0) is normal operation

(9) Output data format (read) from the PLL Chip

Suppose we are input a RF signal of 450KHz to IFIN input, the concerning timing diagram and data output from the CD pin are as follows:

N.B. : The gate time setting now is 16ms.



Since 01C20 (hex) = 7200 (decimal);

By calculation,  $7200 / 16(10^{-3})$

We can restore the frequency value to be 450KHz.

Beware that the data is coming out from the CD at the falling edge of the CK pulses, the 0<sup>th</sup> output bit should be after the 0<sup>th</sup> falling clock edge. That is reason why we have a value of 2 from the second nibble of serial CD data shown above.

Note: the first 20 bits of data are for output counter value and the last 4 bits are for the indication of phase error of the controlled oscillation frequency according to the semiconductor design team information.

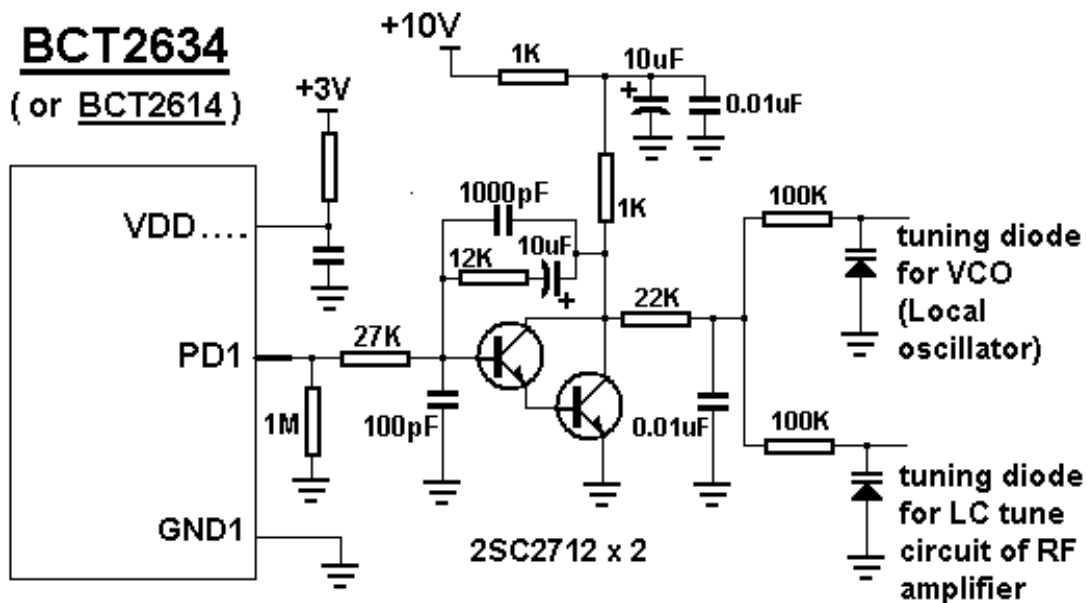
## Application Note

### Phase Comparator output (PD1) and the Loop filter ( Low-pass filter )

The logic operation of the phase comparator is comparing the local output from the divider against the standard frequency programmed by the user.

Logic Output	Phase Comparator Output (PD1)
High	when value obtained by dividing local output is higher than standard frequency
Low	when value is lower
Tri-state	when value is same

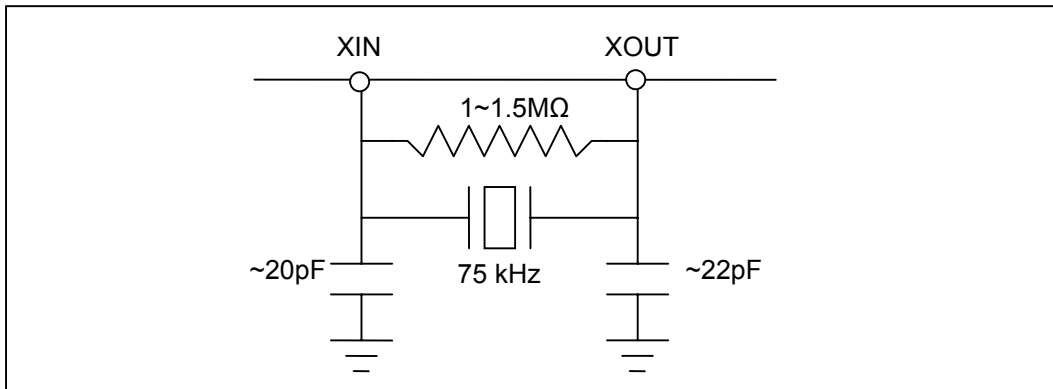
The output of that loop filter delivers DC voltage (average DC level) to bias the tuning diodes so as to track the oscillator frequencies and the tuning frequencies of RF amplifier stages.



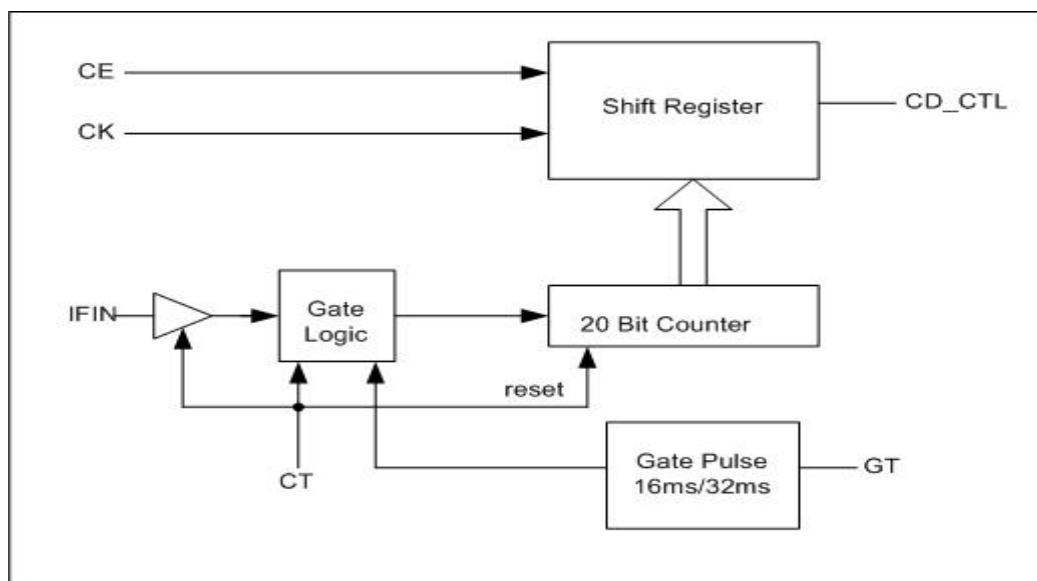
In the above circuit application, we have chosen the standard frequency for FM to be 25KHz and for AM to 3KHz. This loop filter can effectively deliver an average DC voltage to achieve optimal operation between speed and stability. However, different PCB layout design may require further adjustment of those concerning component values for the best performance of the target applications. This circuit has been found to have better signal-to-noise ratio and thus increase the sensitivity by about 3dB.

## Crystal Oscillator

An on-chip crystal oscillator is specially designed with low radiation noise and power consumption in application for radio. An external bias resistor should be connected in parallel with the 75 kHz crystal which should be placed close to the pins XIN and XOUT in the layout. Appropriate values of external bias resistor and capacitors should be referred to the crystal manufactures.

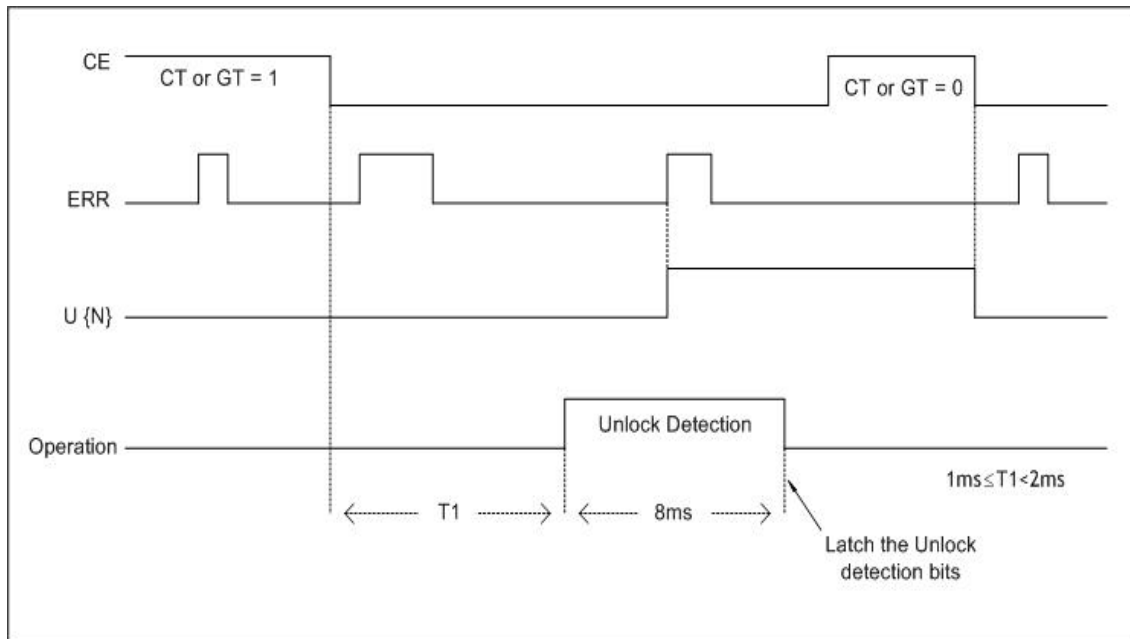


## Intermediate Frequency Counter Operation:



When control data CT equals 1, the 20-bit counter and the IFIN amp go into operation. When CT equals 0, IFIN is deactivated; input pulled down and the counters are reset. Measuring time (gate pulses) is selected (16ms / 32ms) on the basis of control data GT. The value of the IF counter at the end of the measurement period must be read out during the period CT equals 1. This is because the IF counter is reset when CT is set to 0. Bit C0 is LSB and C19 is MSB of the IF Counter.

**Unlock Detection Mechanism:**



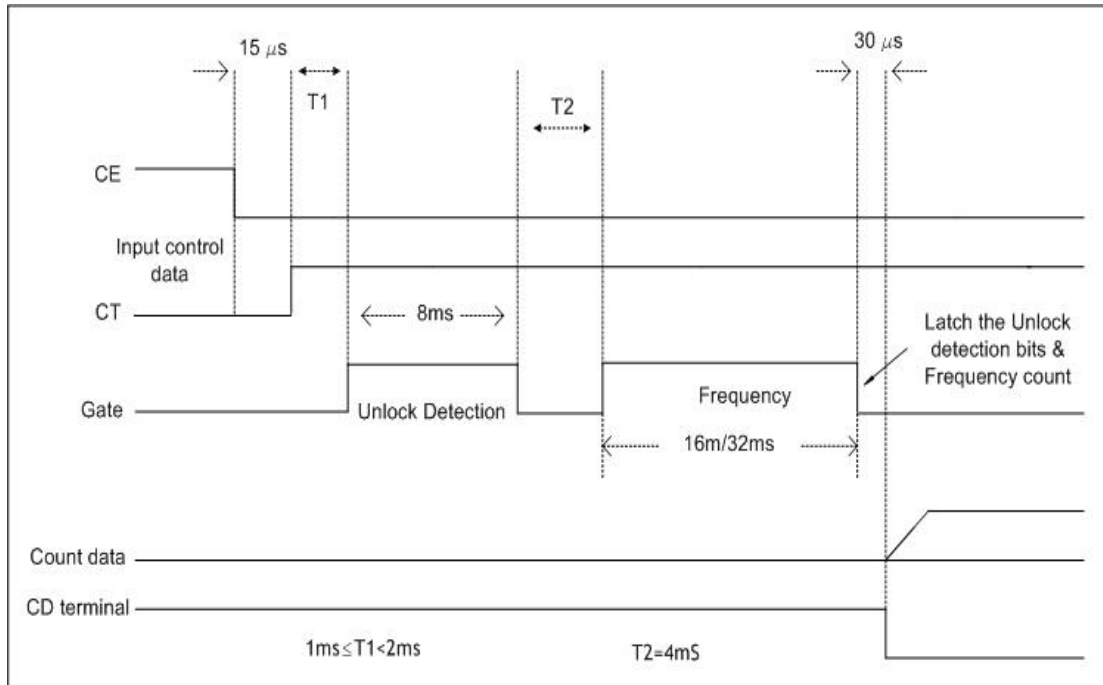
When control data GT equals 1, or CT equals 1, the unlock detection circuit goes into operation for 8ms. When CT equals 1, the unlock detection circuits stops operating before the frequency counter gate pulse is emitted. When CT equals 0 and GT equals 0, the unlock detection circuit is reset.

U0	U1	U2	U3	Phase Error Range
0	0	0	0	$\text{ERR} < 7 \mu\text{S}$
1	0	0	0	$7 \mu\text{S} < \text{ERR} < 13 \mu\text{S}$
1	1	0	0	$13 \mu\text{S} < \text{ERR} < 26 \mu\text{S}$
1	1	1	0	$26 \mu\text{S} < \text{ERR} < 52 \mu\text{S}$
1	1	1	1	$52 \mu\text{S} < \text{ERR}$

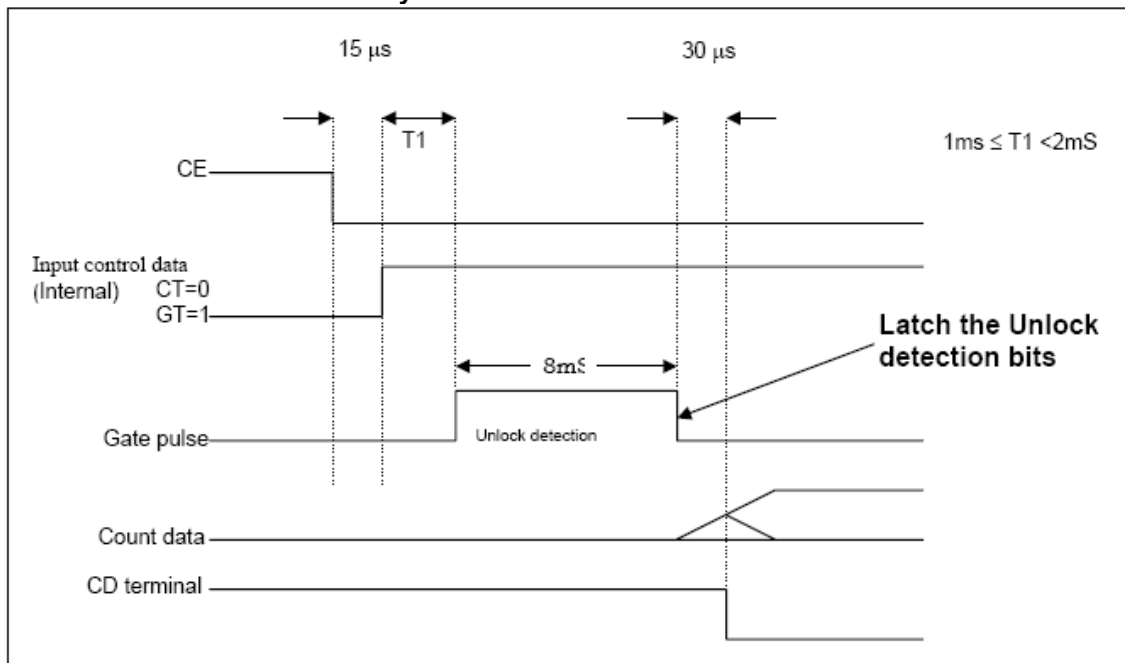
Remarks: These 4 bits are only for indication of the phase error and this function is usually not used in most applications.

**Frequency Counter and unlock Detection:**

1. When CT = 1 : Frequency count and unlock detection are carried out.

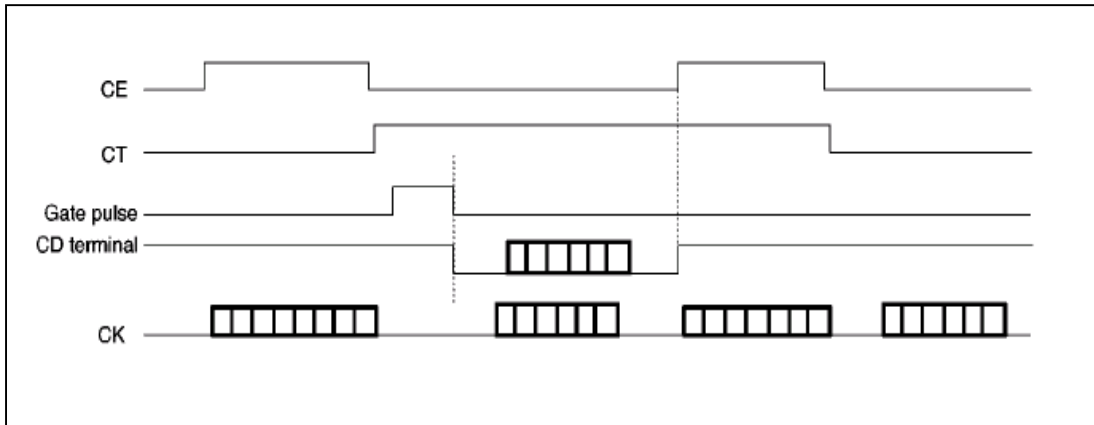


2. When CT = 0 and GT = 1: Only unlock detection is carried out.



## Explanation of CD Terminal

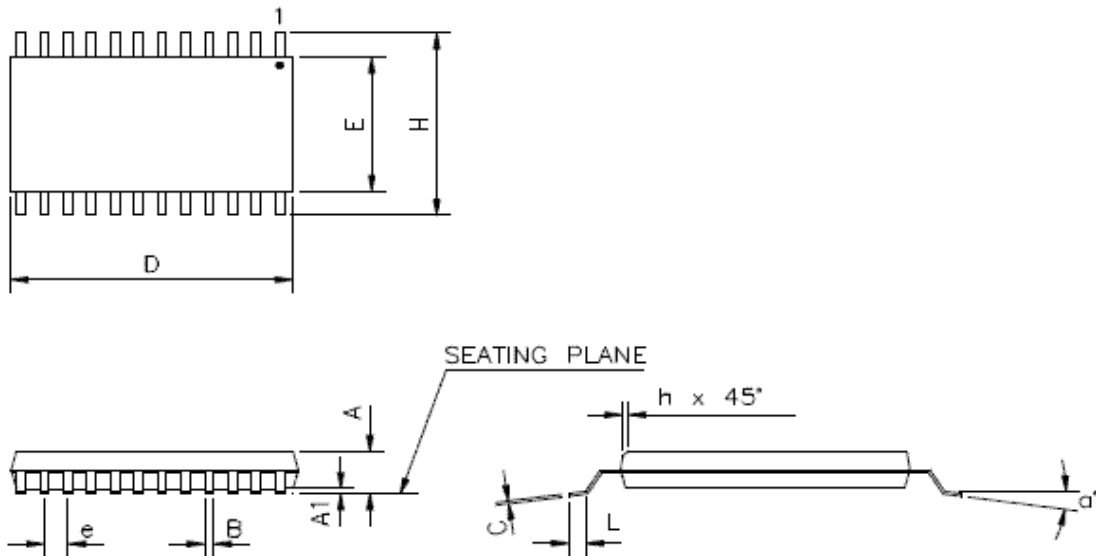
When frequency measurement or unlock detection is finished, the CD terminal goes to Low to indicate that the count and unlock detection have finished. It also synchronizes with CK to output counter data. When the next data is input, it goes to High.



Originally written by : TW Cheung (in 2006)

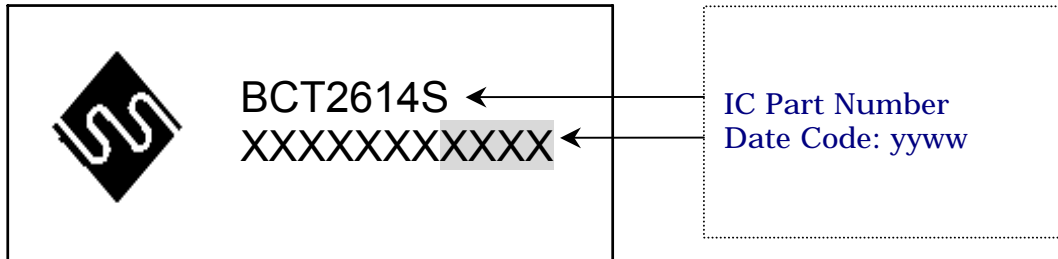
Modified and updated by : Man Lo (in 2007)

## SO16 Dimensions



SYMBOL	MIN (Inch)	MAX (Inch)
A	0.060	0.068
A1	0.004	0.008
B	0.014	0.019
C	0.007	0.010
D16	0.386	0.394
E	0.150	0.157
e	0.050 BSC	
H	0.230	0.244
h	0.010	0.016
L	0.016	0.035
$a^\circ$	$0^\circ$	$8^\circ$

## Marking Notation / Ordering Information



## Sales Offices

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