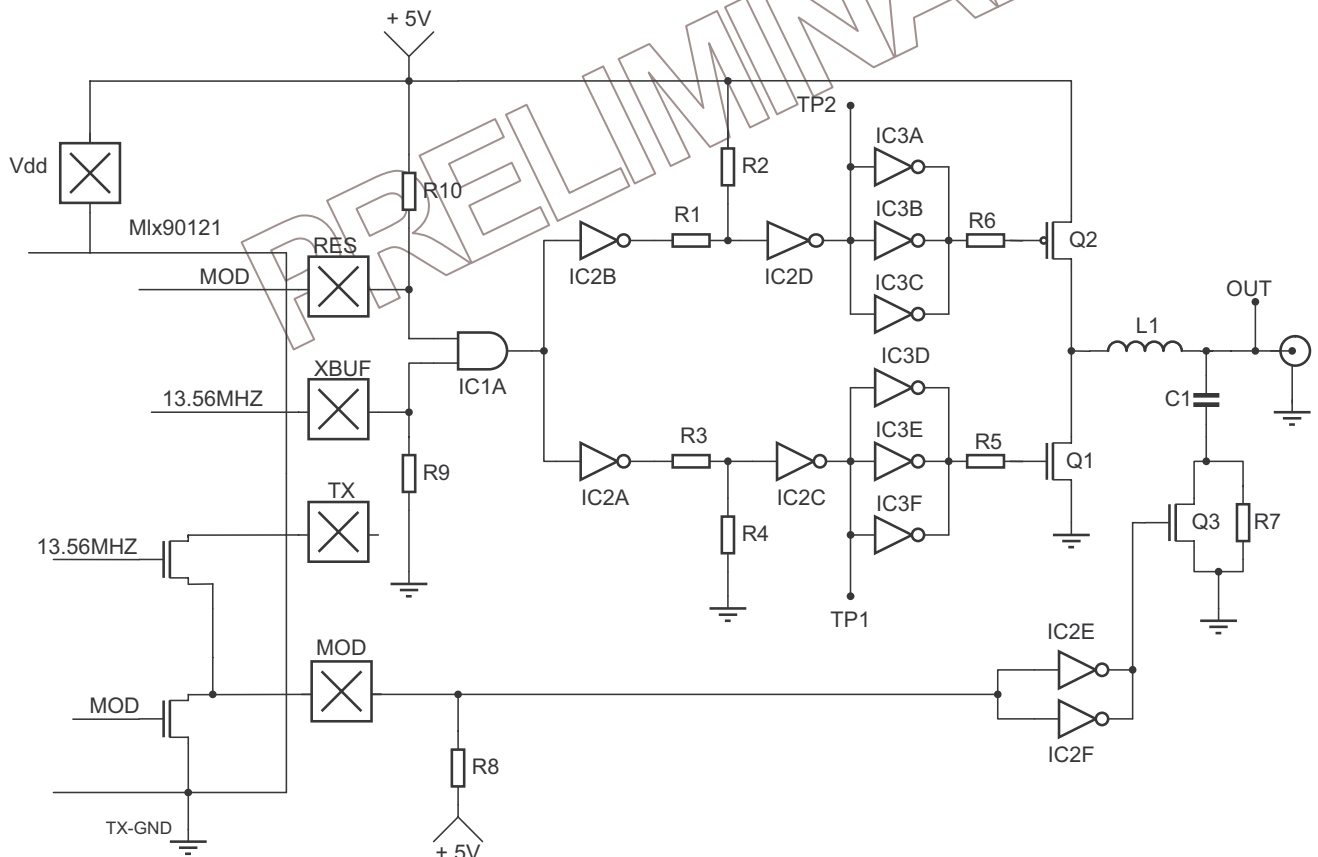


1 Scope:

For some applications, single supply operation is a must. In this document, an 1 Watt power booster for the MLX90121, that requires only a single 5 volts power supply, is described. Only standard CMOS high speed logic is required to generate the drive signal to the power stage, which is in fact a high power CMOS inverter. Furthermore, the output matching circuit can be reduced to a bare minimum of two components, reducing circuit complexity and cost.

2 Application schematic:



2.1 Recommended Components:

Reference	Value	Comments
R1,R2,R3,R4	See text	
R5, R6	4.7 ohms	5% or better
R7	See text	
R8	2.2 K ohms	5% or better
R9, R10	10 K ohms	5% or better
C4	5-50 pF variable	100Volts
IC1	74 AC 08	
IC2, IC3	74 AC 04	
Q1, Q2, Q3	FDC 6327C	FAIRCHILD
L1	130 nH	See note 1
C1	1 nF	See note 2

Notes:

1) Minimum current rating: 1 Amp.
Recommended component is [COILCRAFT](#) "Maxi Spring" part number 132-11SM.

2) Use only a very low loss capacitor. Current rating is the same as L1. A MICA capacitor is recommended. ([Cornell Dubilier](#), [Arco](#)). If you prefer ceramic, you can purchase low loss RF ceramic power caps from [ATC](#).

3 Theory of operation and design guidelines:

3.1 Theory of operation.

In order to reduce the current drain to a minimum, we do not use the power stage of the MLX90121. Instead, we take advantage of the clock output (XBUF, pin 8). From this point, we generate two independent drive signals that will be used by the final power inverter formed by the complementary pair Q1, Q2. Components R1, R2, R3, R4, are used to define the duty cycle of the signals applied to the gates of the PMOS transistor Q1 and the NMOS transistor Q2, respectively. This configuration creates a non-overlapping gate drive for the transistors Q1 and Q2, avoiding excessive power dissipation. By adjusting independently the duty cycle of the drive signal applied to each gate, we can fine tune the amplifier to obtain the best power efficiency.

Three 74AC04 gates are connected in parallel to generate for each power FET the gate drive. Use of the 74AC family is required as it has enough fan-out to directly drive the gates of Q1 and Q2 that have a fairly large capacitance. (about 330 pF)

R5 and R6 are connected in series with the gates. This reduces slightly the overall efficiency, but it avoids parasitic oscillations. The optimal resistor value is layout dependent; some kind of fine tuning could be required.

The output matching circuit is implemented by L1 and C1. Together, they form a low- to high impedance converter. L1 and C1 must have very low losses. L1 sees an AC current of about 2 Amps peak-peak. When substituting the recommended L1 from Coilcraft by some other component, you have to take care of its current rating. The same holds true for C1.

In order to meet applicable electromagnetic compatibility standards, an additional low pass filter maybe required.

Modulation in 100% mode is achieved by using a special output pin (RES, pin 18) of the MLX90121 from which modulation pulses can be recovered. For info on how to configure the MLX90121 to do this, please contact Melexis. These pulses are applied to the 74AC08 gate to key the carrier on and off. R10 is a pull up resistor that makes sure that when the RES pin goes to a high impedance state, the carrier from XBUF still drives the amplifier. R9 is a pull down intended to make sure that when the carrier is off, the DC voltage at the output antenna connector is 0 volts. Please note that the antenna output is DC coupled. This is not a problem since most RFID antennas have a DC blocking cap somewhere in the signal path. To check the signal power on a dummy load (50 ohms resistor), one must insert a DC blocking capacitor in series with the output. Two high quality plastic film 47 nF capacitors placed in parallel will do the job.

Low index modulation is achieved by means of an additional power MOSFET Q3. Since the normal output power stage of the MLX90121 is unused, the RMOD output is pulled-up with resistor R8 to Vcc, generating a modulation signal. The value of the pull up resistor has to be kept low enough so that capacitance does not become a problem. A value of 2.2 K gives good results. Two 74AC04 inverter gates are used to drive the gate of Q3 and provide the proper signal polarity. The value of R7 will be layout dependent. One should start to experiment with a value of 1 ohm. A tight tolerance is required (1% or better). The power rating of R7 should be no less than 500 milliwatts.

3.2 Fine tuning of the circuit.

If you plan to use your own layout, some adjustments may be required. The trickiest point is to set the correct value for the duty cycle of each gate. In the first place, one should replace R1, R2, R3, and R4 by two multi turn potentiometers. The lowest possible value must be used for the pot. High ohmic values will dramatically increase the rise and fall times, because of the 74AC04 gate input capacitance. We suggest to use a 2K pot from the BOURNS 3296W series.

To adjust the duty cycle, remove R5 and R6 from the board, tie the PMOS gate to VCC (+ 5 volts) through a 1K resistor, tie the NMOS gate to GND through a 1K resistor, and adjust the duty cycle for each gate to 80%/20% and 20%/80% respectively. Remove the two 1K resistors, put back in place R5 and R6. Monitor at the same time the duty cycle at each gate, the output voltage on an adequate dummy 50 ohms load, and the power supply current. Increase little by little the duty cycle on each gate until the output voltage stops increasing. Go back a little to make sure that you have the best power efficiency. Check the current drain, the power output, and verify Q1 and Q2 power dissipation. Although the FDC6327C case is rated for 1 Watt at 25°C, we recommend having no more than 0.5 Watts total power dissipation for Q1, Q2.

The logic circuits may have slightly different characteristics, depending on their manufacturer. It is best to use only one manufacturer for all the gates. In case of substitution, check again the duty cycle settings.

Use adequate decoupling whenever possible. Place decoupling caps close to the power pins of each IC. Use good quality caps, some ceramic caps have unacceptable ESR values. Most manufacturers provide models and/or simulation tools that let you examine the frequency characteristics of their products. Since we have very fast edges in the circuit, it will be necessary to have a combination of several capacitors to have a proper decoupling at all the frequencies of interest. A low ESR tantalum cap will provide the general low frequency decoupling. For each IC power pin, a 100 nF in parallel with a 100 pF is a good combination. Additionally, the use of RF chokes to isolate the different supply rails is highly recommended. These chokes should have the highest possible resistive component, since this is the best way to prevent ringing and "communication" between the circuits via the supply rails.

Note: One should plan in advance adequate test points for the gate drive signals. The best is to have test points where you can plug the scope probe head directly, thereby insuring the best possible monitoring. Using a standard probe ground attachment is NOT an acceptable option. Inductance does matter a lot. If you cannot use specific probe head inserts, the following trick may work. Take a piece of small gage rigid wire. Form a coil spring around the scope probe head where you will find in general the ground connection. Twist both ends on a SHORT length (less than 1.5 centimeters). Solder directly on the ground plane close to the pcb trace you want to monitor the resulting ground attachment. The only requirement is to have planned a plated through hole in the middle of the pcb trace with a drill diameter large enough to accommodate the probe tip pin. Be careful to not break the probe tip!

It is recommended to have the antenna close to the transmitter, by preference on the same board. If this is not possible a 50Ohm coax cable may be used, but care must be taken to the cable length as matching is not a perfect 50Ohm. Performance might then be cable length dependent.

3.3 Printed circuit board layout issues.

The track length between R5, R6 should be kept to an absolute minimum. The same holds true for the tracks that go from the 74AC04 gates to these resistors. If some length cannot be avoided, the trace should be as wide as possible. The width of a 0805 resistor is a minimum. One must always remember that in this application, stray inductors and ringing are the enemies. If too much ringing occurs at the power MOSFETS gates, they may turn on simultaneously. This will affect severely the amplifier efficiency or even destroy it. Use of large ground plane is an absolute necessity. However, it is best to think and plan in advance where the return currents will flow. We are not in the microwave range of frequencies, and it is perfectly acceptable to insert slits in the ground plane in order to channel the return currents paths, and create areas where the ground plane is quiet.

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